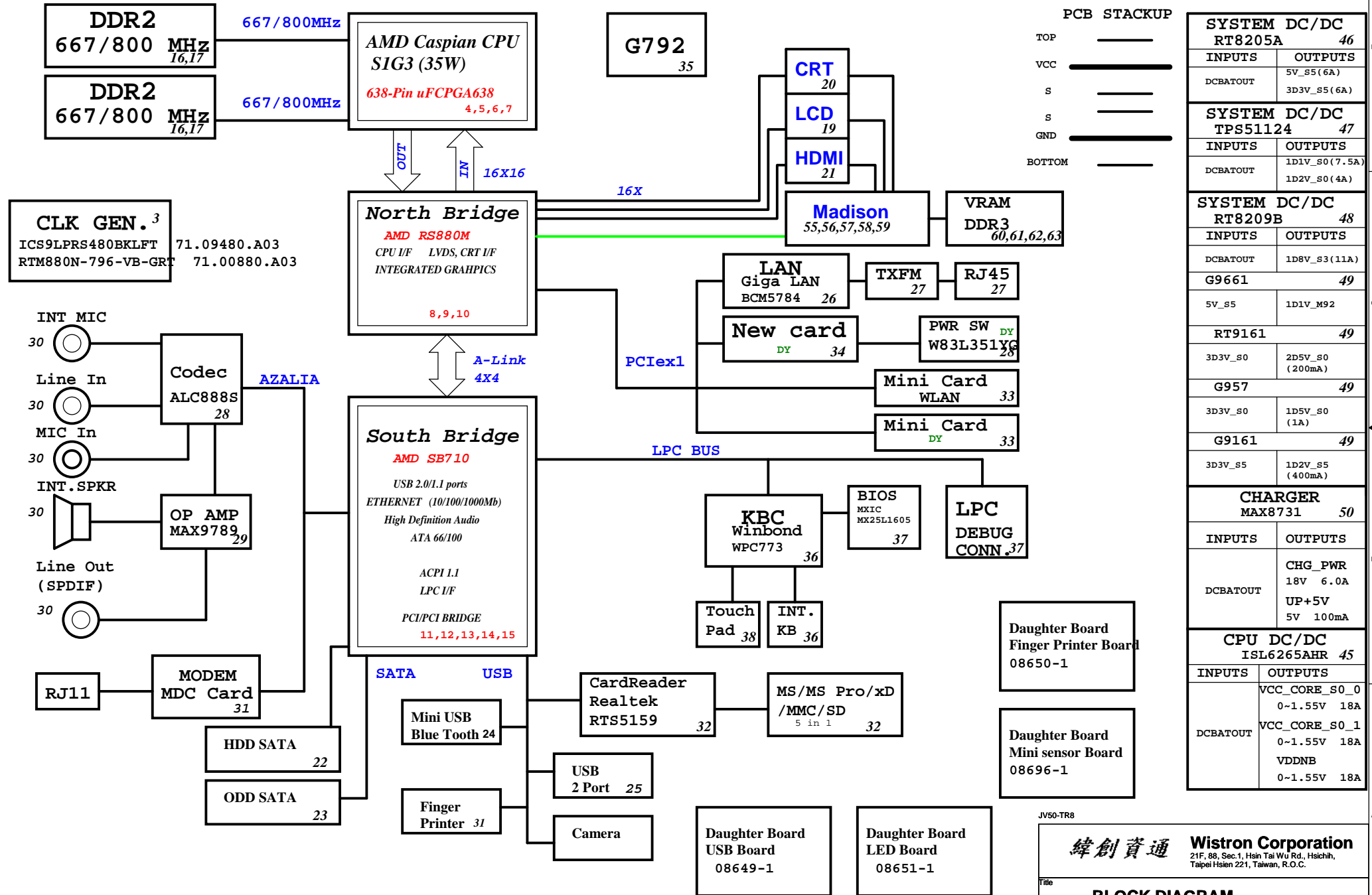


JV50-TR_8VRAM Block Diagram

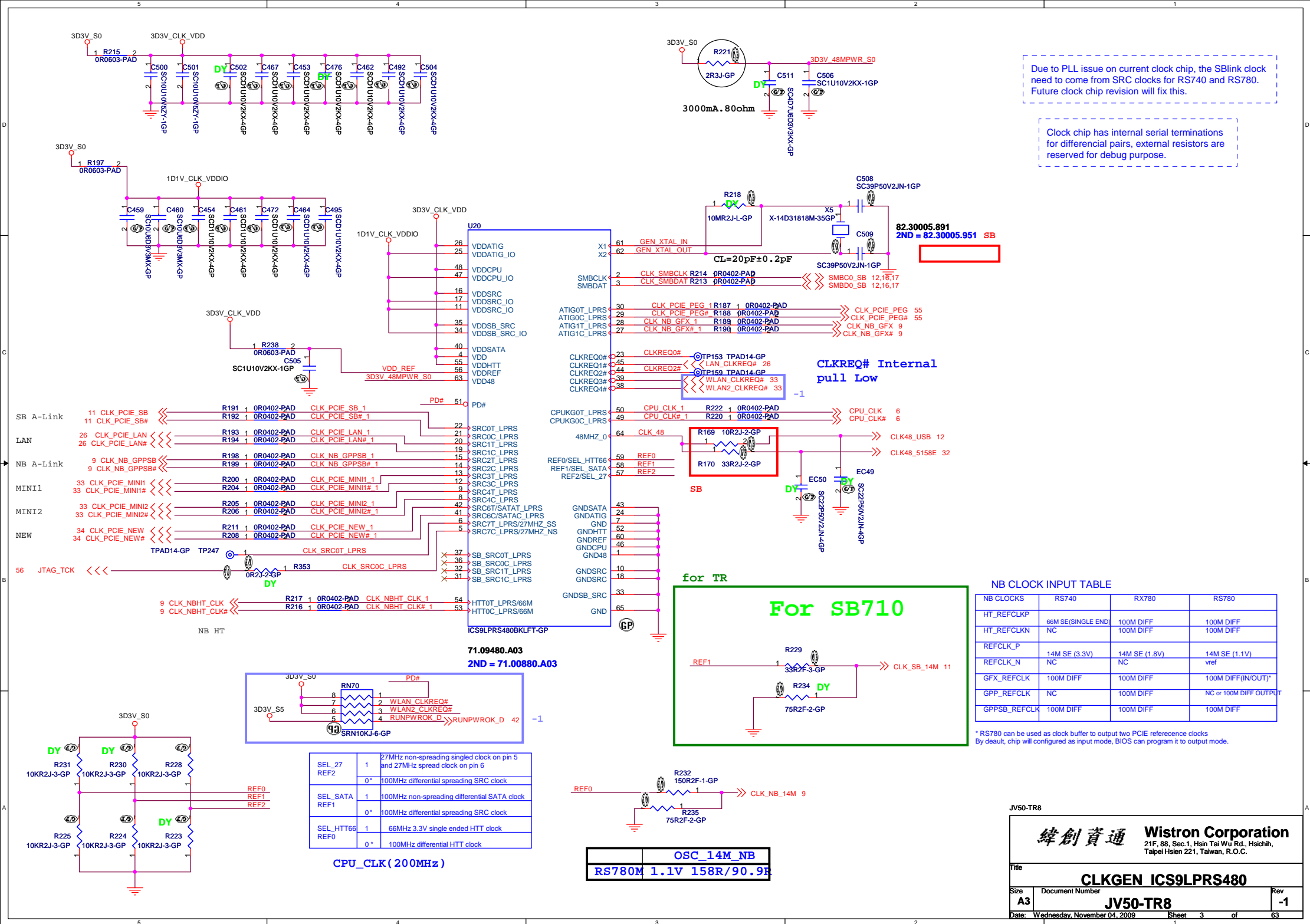
PCB P/N : 48.4FN02.001

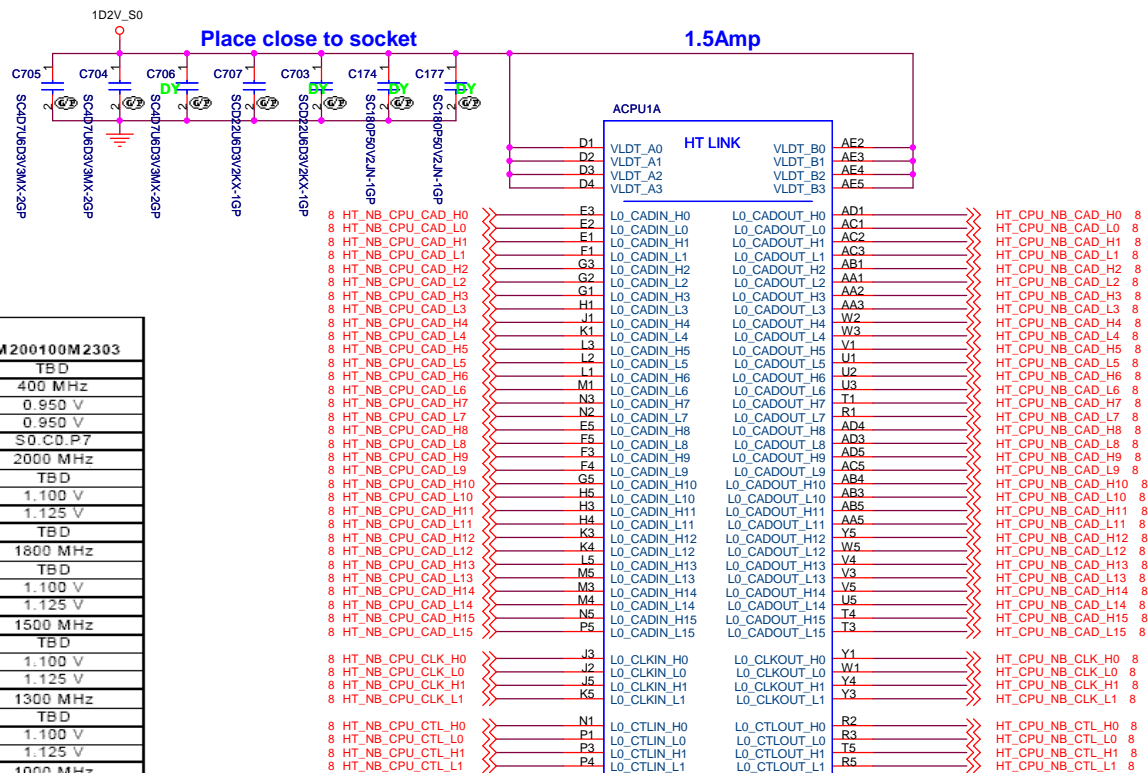
REVISION : 09927-1



JV50-TR8

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
USB/PCIE Routing		
Size	Document Number	Rev
A3	JV50-TR8	-1
Date:	Monday, October 05, 2009	Sheet 2 of 63





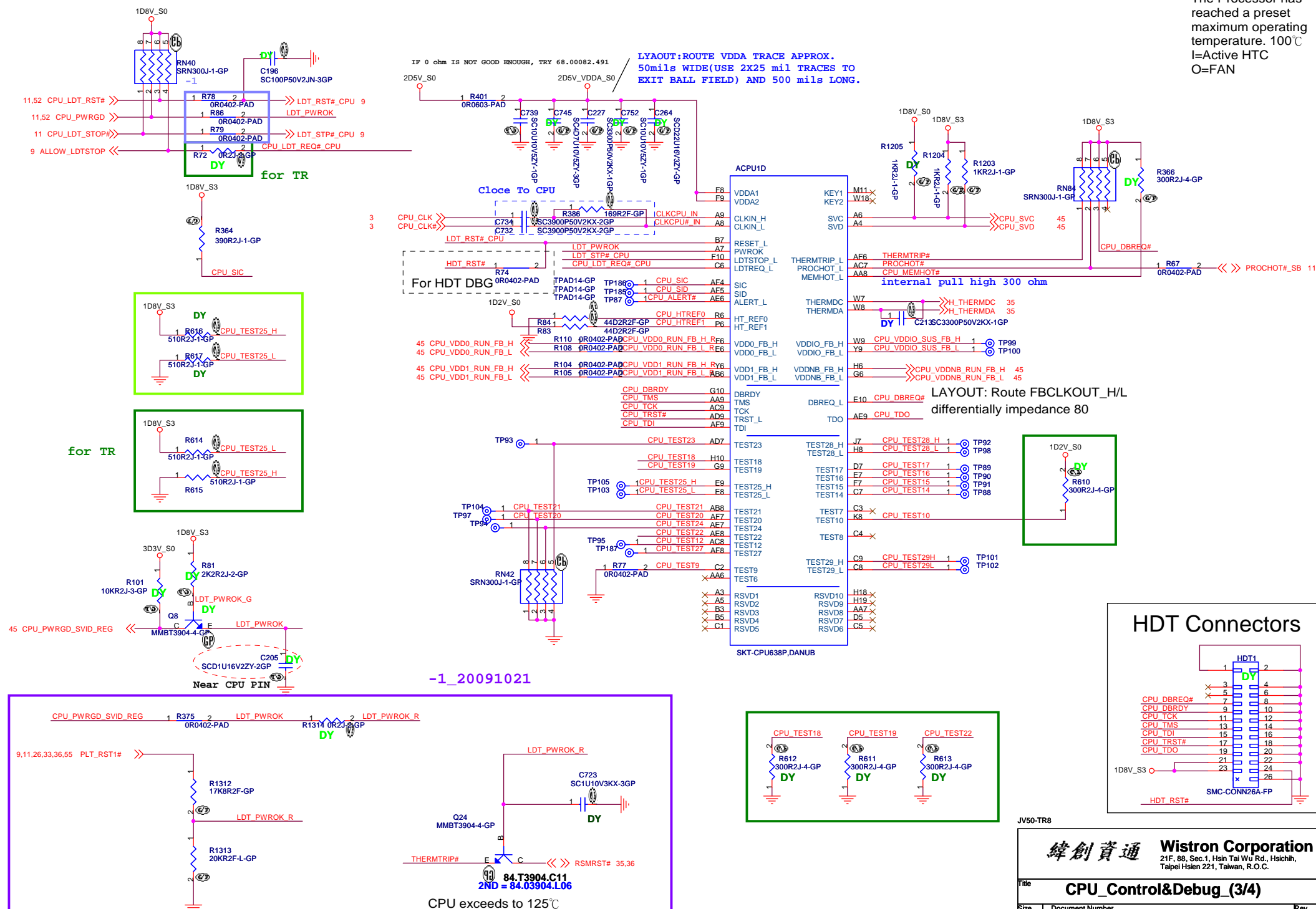
State	Specification	Notes	ZM200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1500 MHz
S0.C0.P2	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1300 MHz
	TDP	3	TBD
S0.C0.P3	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
S0.C0.P4	VID_VDD Max	2	1.125 V
	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
S0.C0.P6	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
S0.C0.P7	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V

SKT-CPU638P.DANUB
62.10055.111
2ND = 62.10055.251
SKT-BGA638H176

JV50-TR8

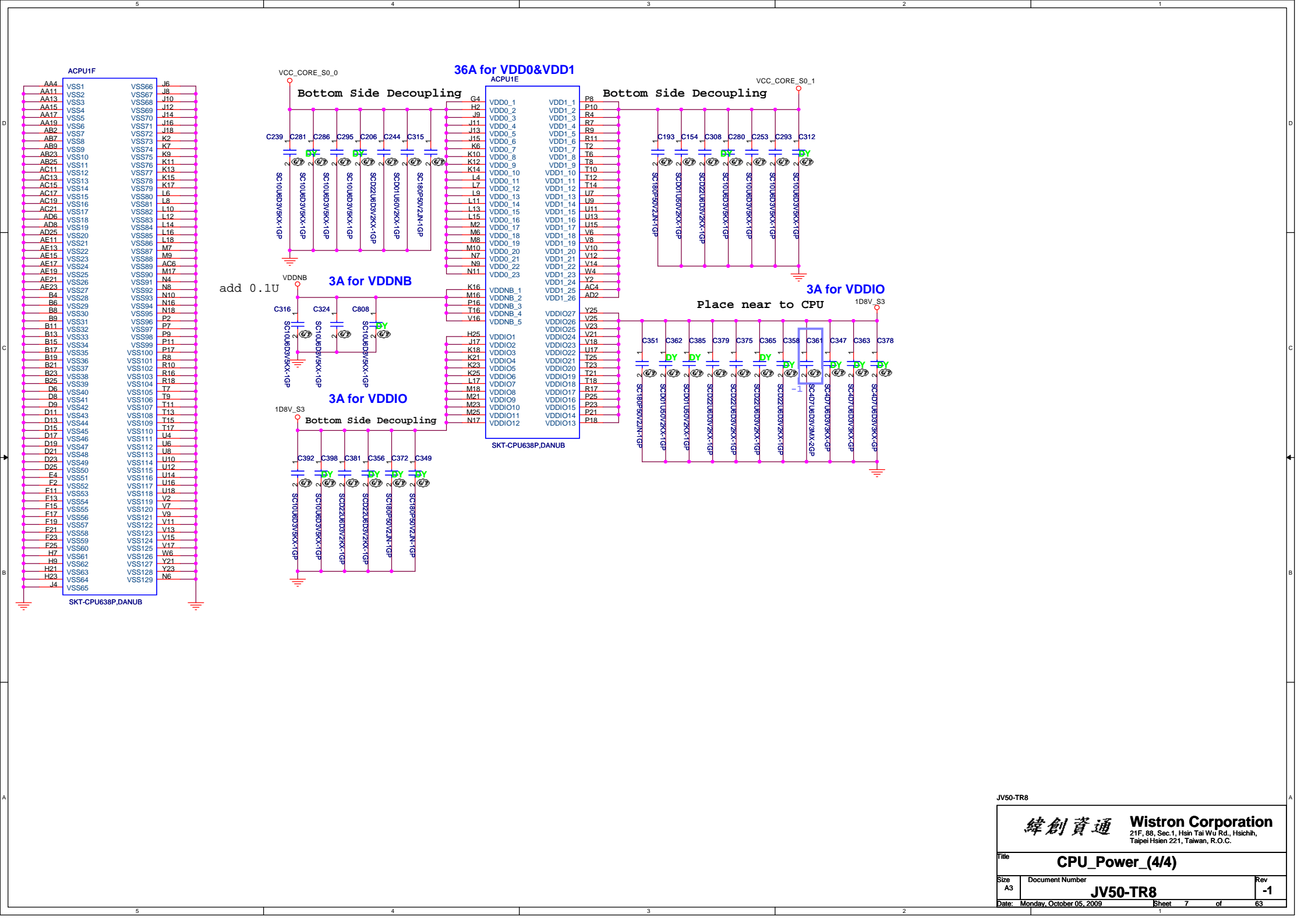
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CPU HT LINK I/F (1/4)			
Size	Document Number	Rev	
A3	JV50-TR8	-1	
Date:	Monday, October 26, 2009	Sheet	4 of 63

The Processor has reached a preset maximum operating temperature. 100°C
I=Active HTC
O=FAN

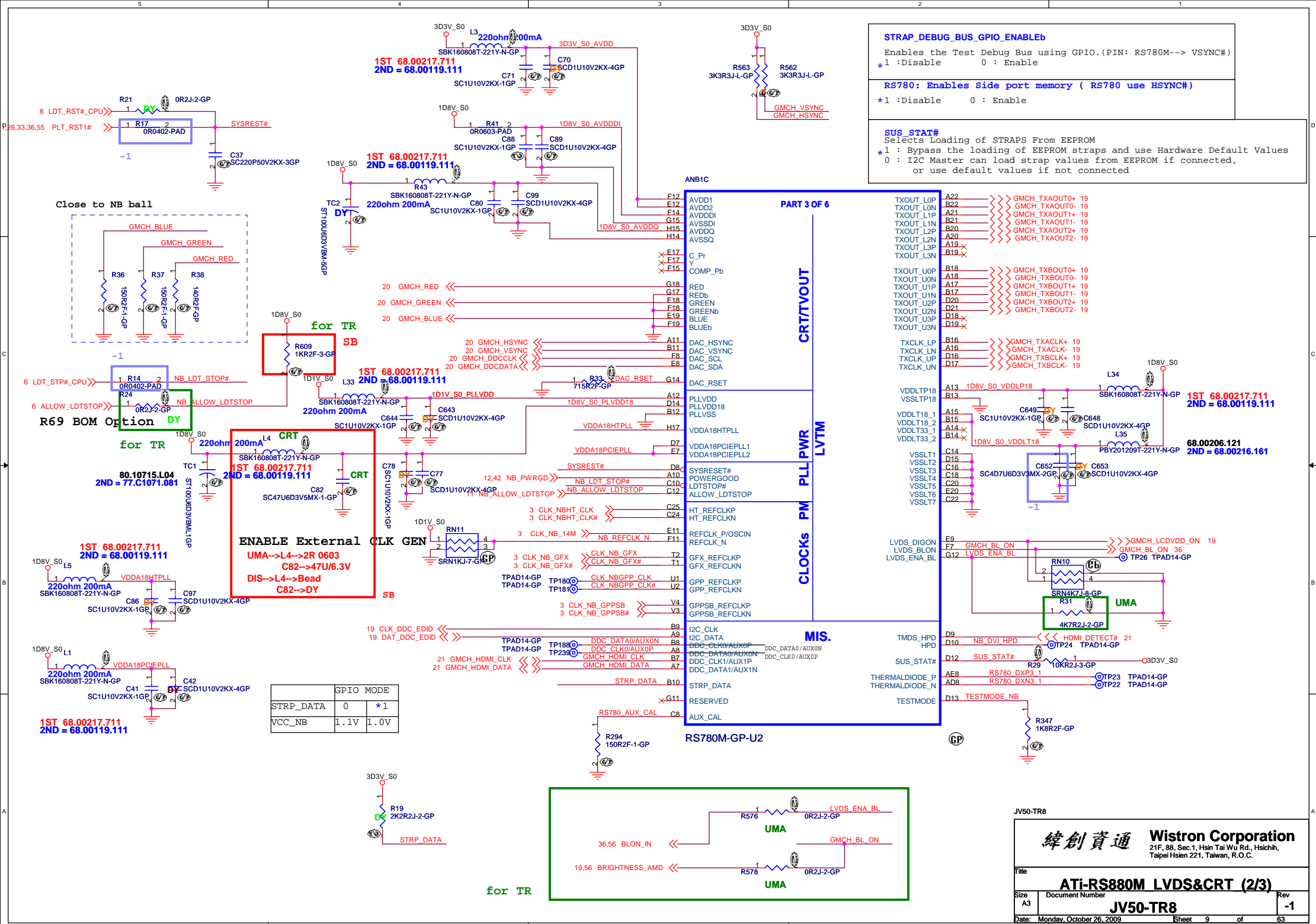


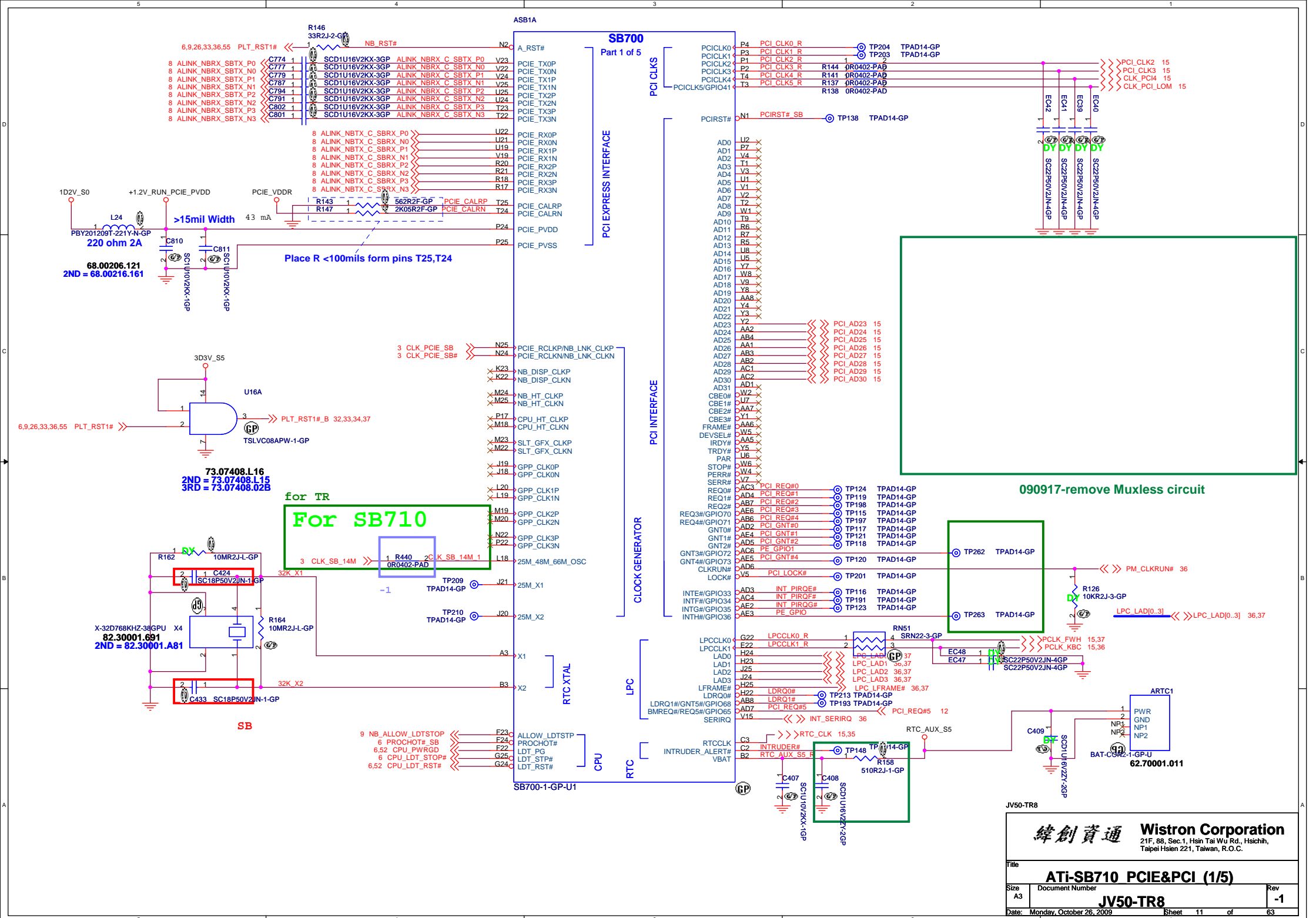
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

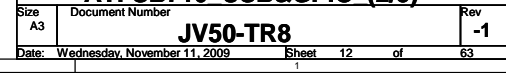
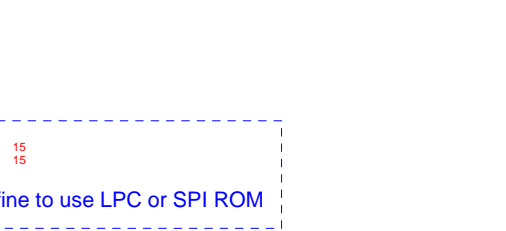
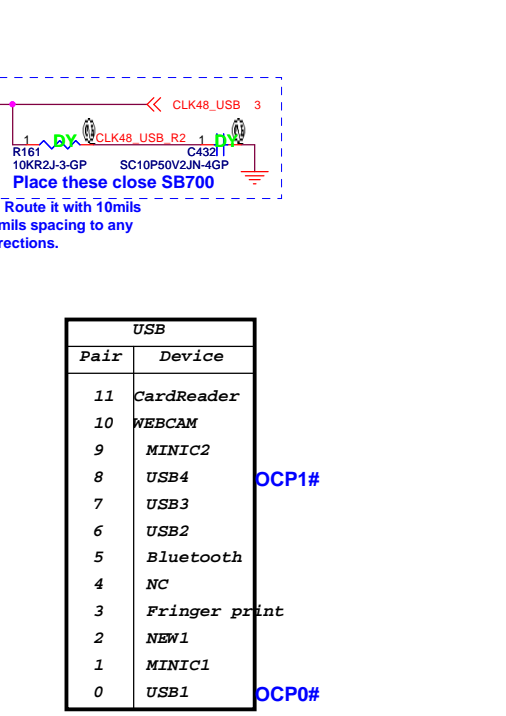
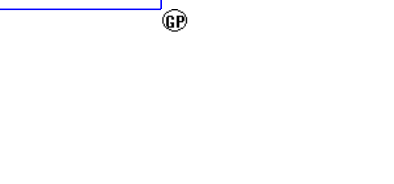
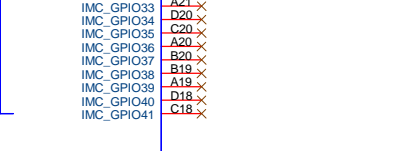
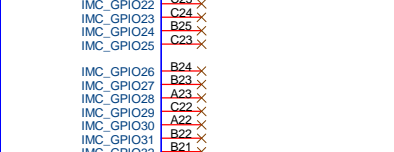
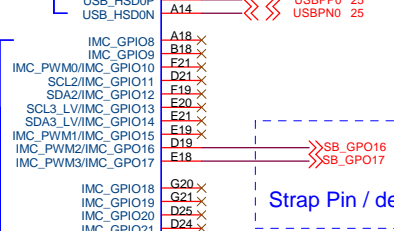
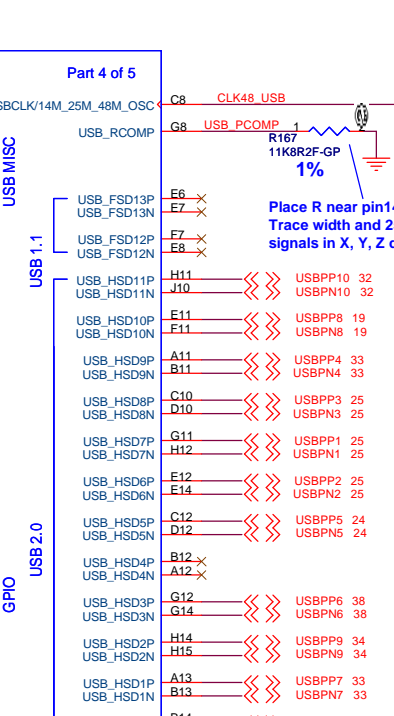
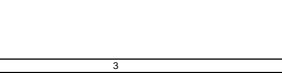
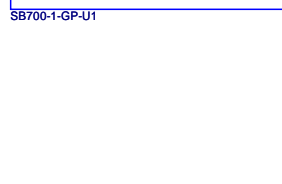
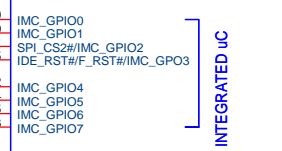
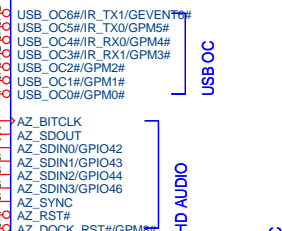
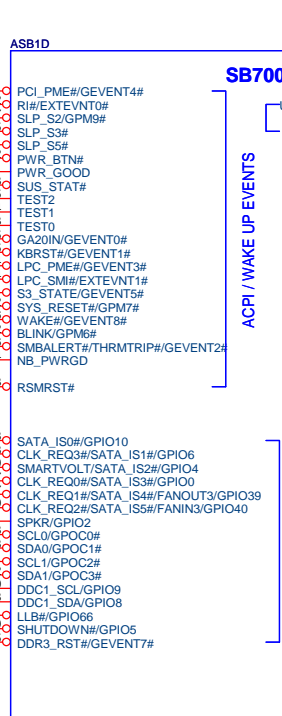
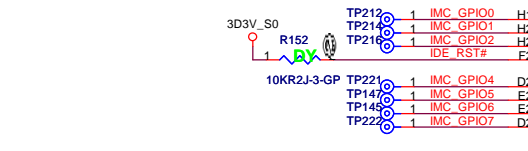
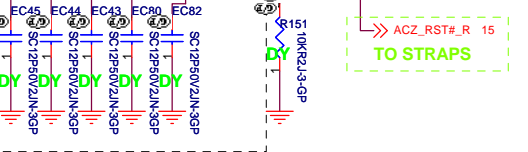
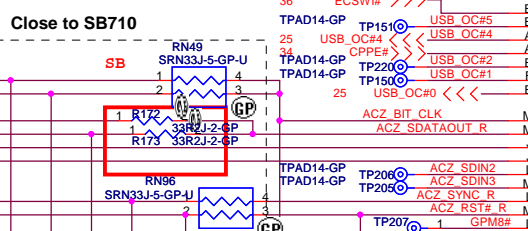
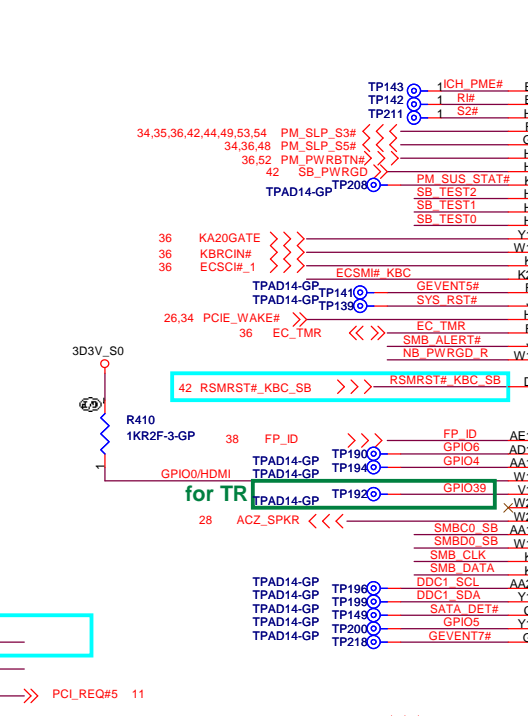
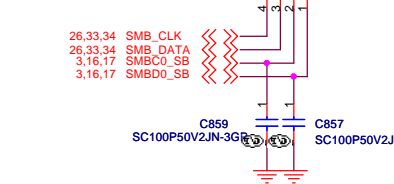
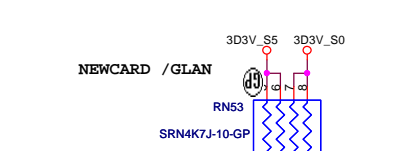
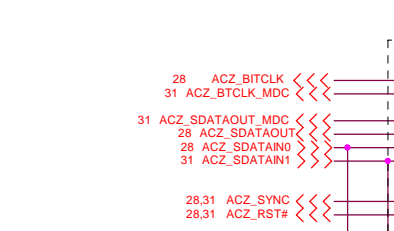
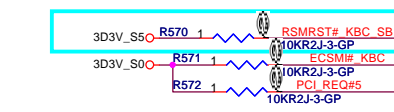
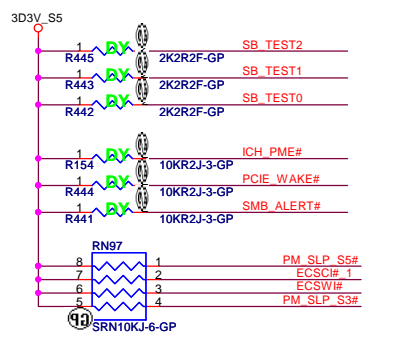
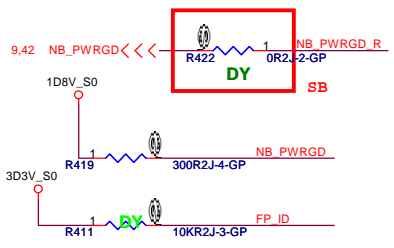
Title				CPU_Control&Debug_(3/4)			
Size	Document Number						Rev
A3	JV50-TR8						-1
Date:	Monday, October 26, 2009				Sheet	6	of 63



JV50-TR8







USB	
Pair	Device
11	CardReader
10	WEBCAM
9	MINIC2
8	USB4
7	USB3
6	USB2
5	Bluetooth
4	NC
3	Fringier print
2	NEW1
1	MINIC1
0	USB1

OCP1#

OCP0#

Place R near pin14. Route it with 10mils

Trace width and 25mils spacing to any

signals in X, Y, Z directions.

Place these close SB700

Place these close SB700

Place these close SB700

Place these close SB700

Place these close SB700

Place these close SB700

Place these close SB700

Place these close SB700

Place these close SB700

Place these close SB700

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Place these close SB700

Place these close SB700

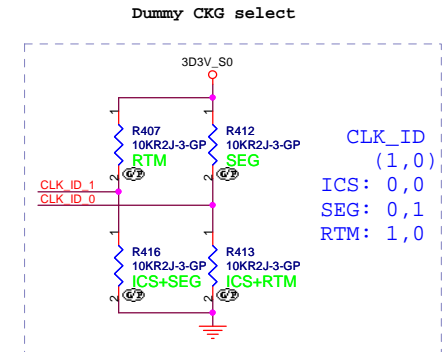
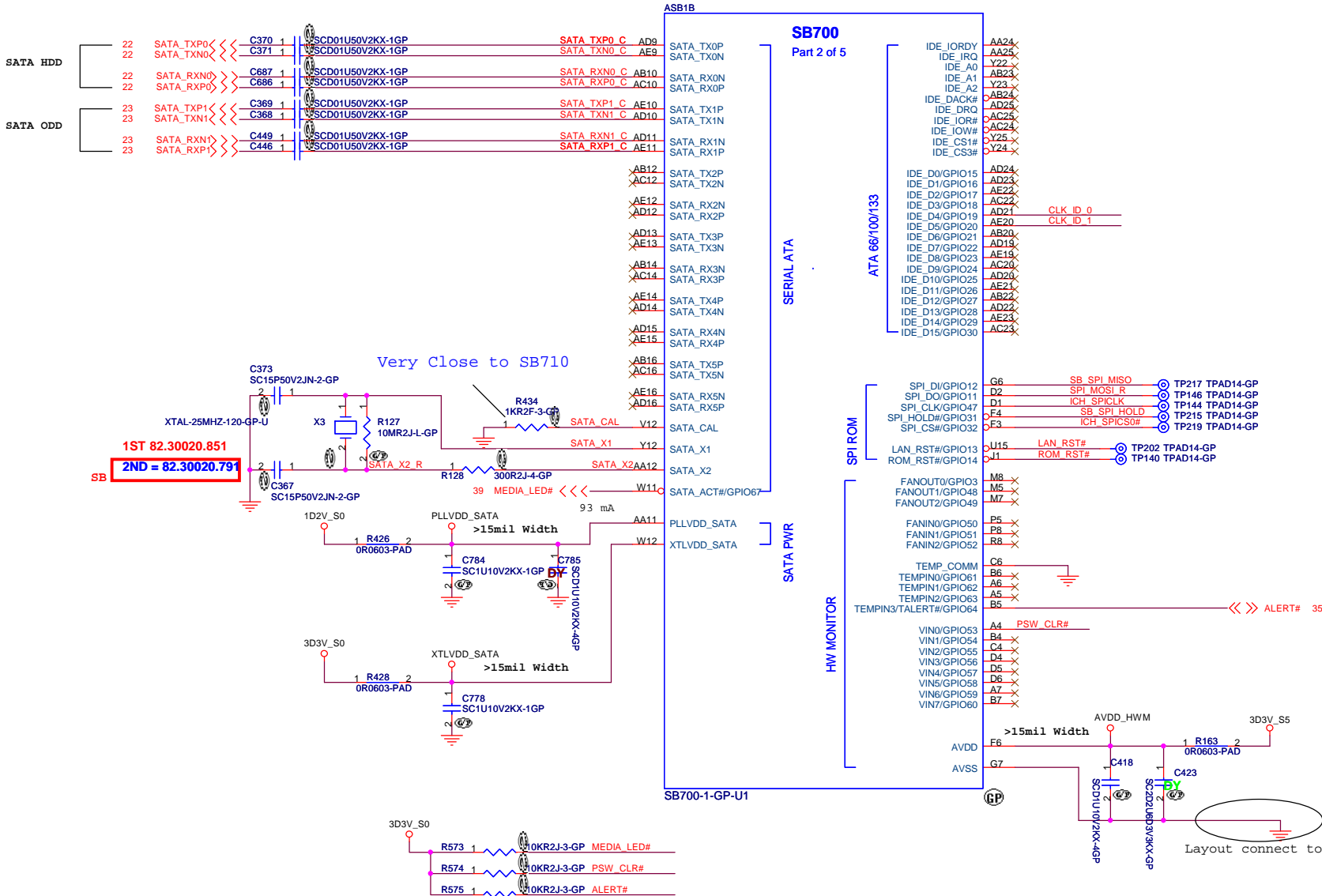
Place these close SB700

Place these close SB700

Place these close SB700

Place these close SB700

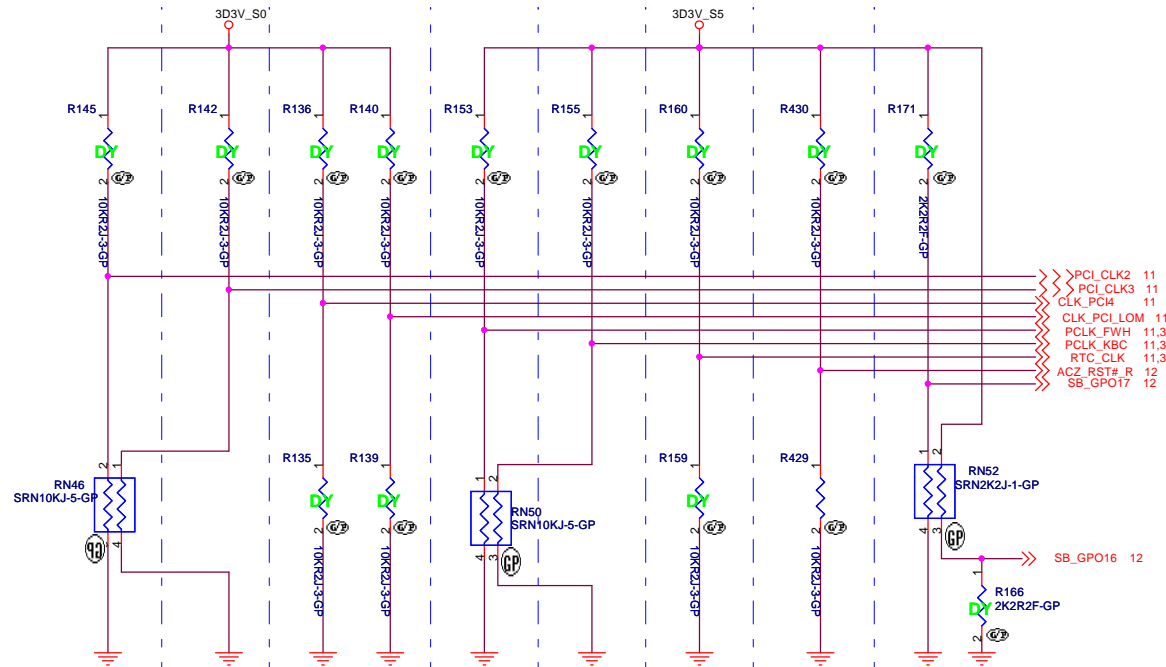
PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB710



JV50-TR8

REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



DEBUG STRAPS

TPAD14-GP	TP137	PCI_AD23	11
TPAD14-GP	TP136	PCI_AD24	11
TPAD14-GP	TP195	PCI_AD25	11
TPAD14-GP	TP135	PCI_AD26	11
TPAD14-GP	TP134	PCI_AD27	11
TPAD14-GP	TP133	PCI_AD28	11
TPAD14-GP	TP130	PCI_AD29	11
TPAD14-GP	TP129	PCI_AD30	11

	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17, SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

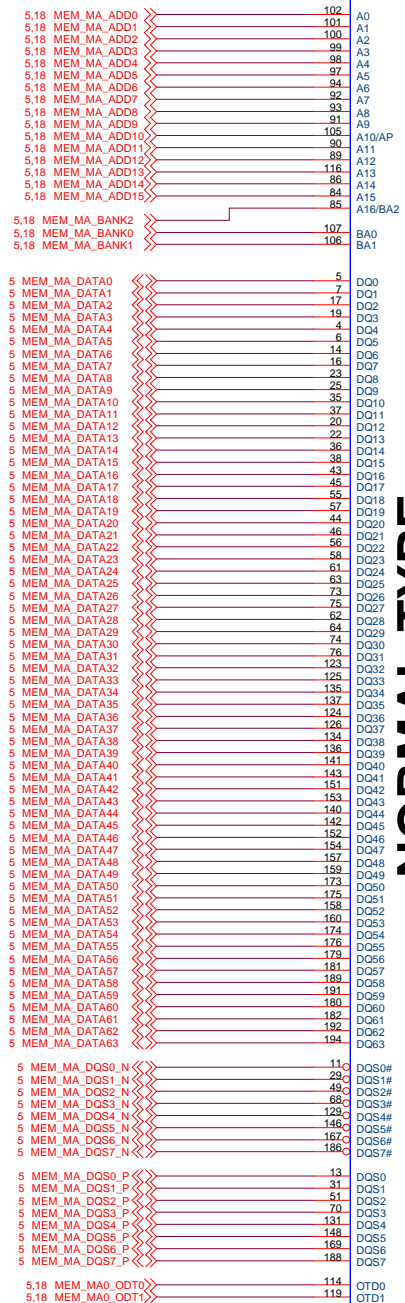
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

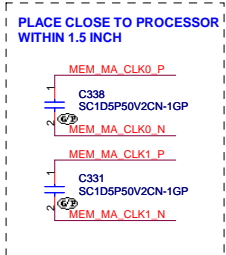
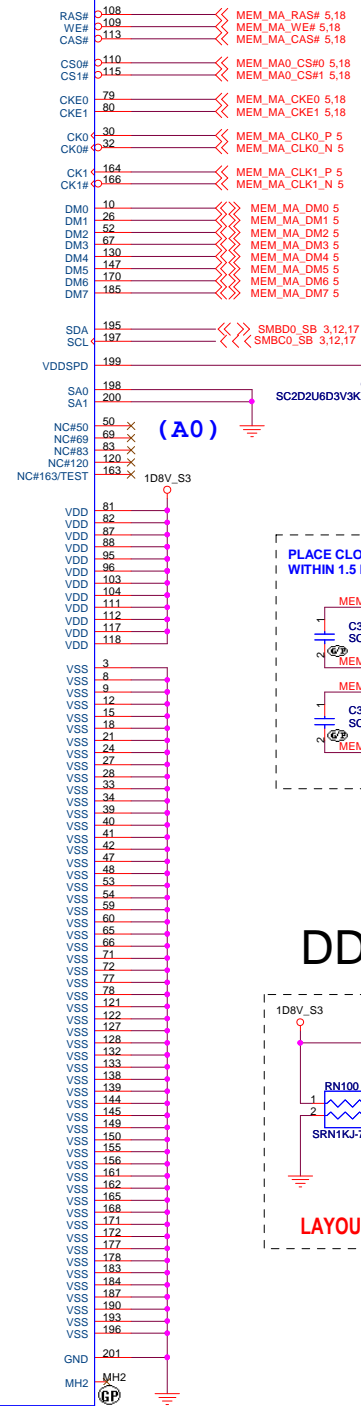
JV50-TR8

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

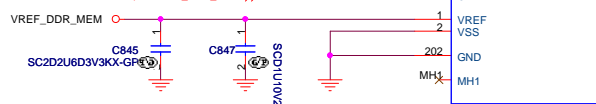
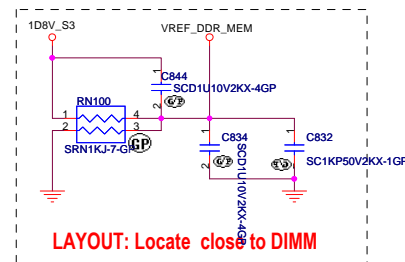
Title ATI-SB710 STRAPPING (5/5)		
Size A3	Document Number JV50-TR8	Rev -1
Date: Monday, October 26, 2009 Sheet 15 of 63		



NORMAL TYPE



DDR_VREF



Place C2.2uF and 0.1uF < 500mils from DDR connector

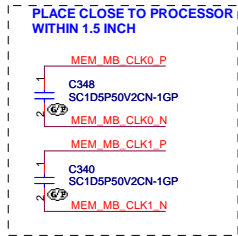
2ND = 62.10017.A41
3RD = 62.10017.G81

LOW 5.2 mm

WWW.AliSaler.Com

JV50-TR8

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
DDR_SO-DIMM SKT 1	
Size	Document Number
Custom	JV50-TR8
Date: Monday, October 26, 2009	Sheet 16 of 63

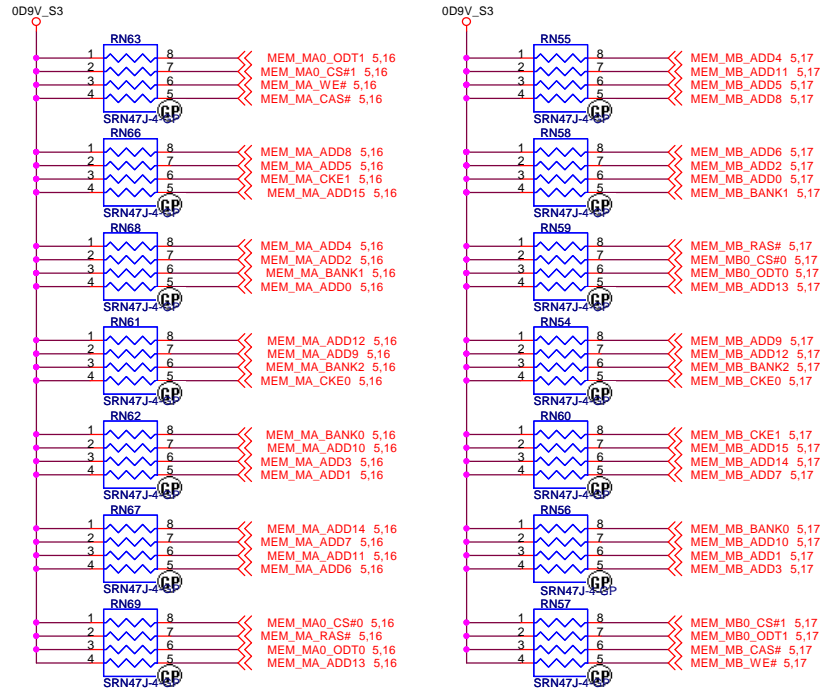


NORMAL TYPE

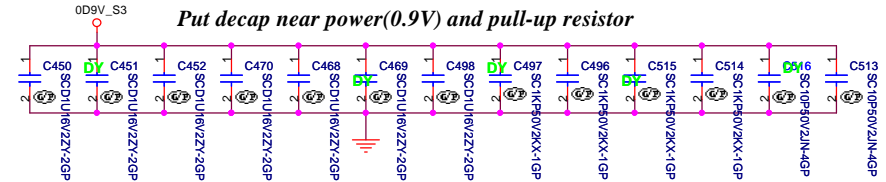
Place C2.2uF and 0.1uF < 500mils from DDR connector

PARALLEL TERMINATION

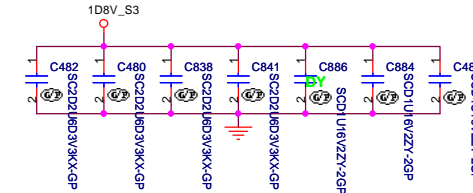
Put decap near power(0.9V) and pull-up resistor



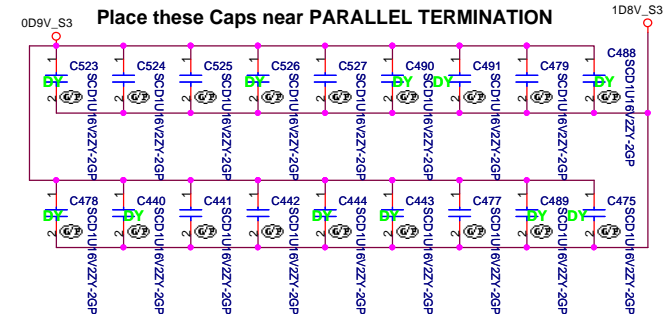
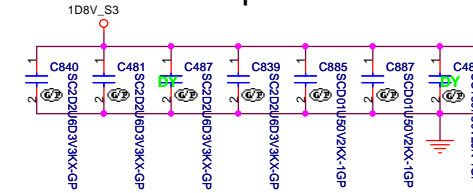
Decoupling Capacitor



Place these Caps near DM1



Place these Caps near DM2

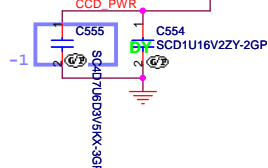
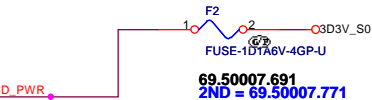
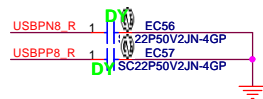
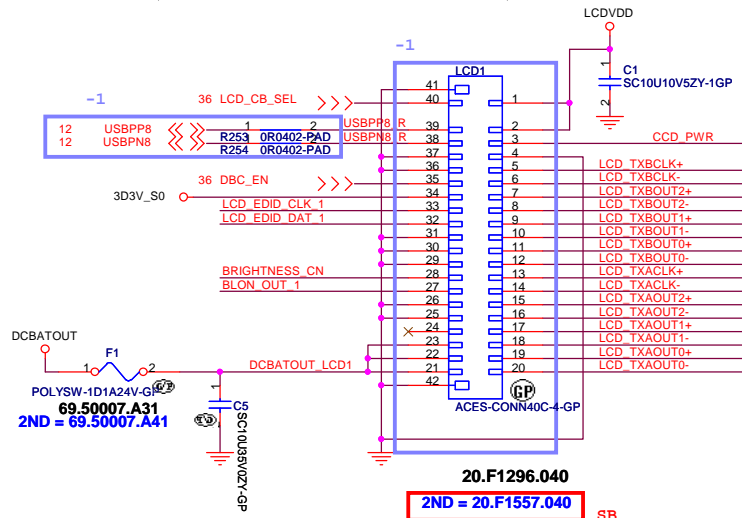


JV50-TR8

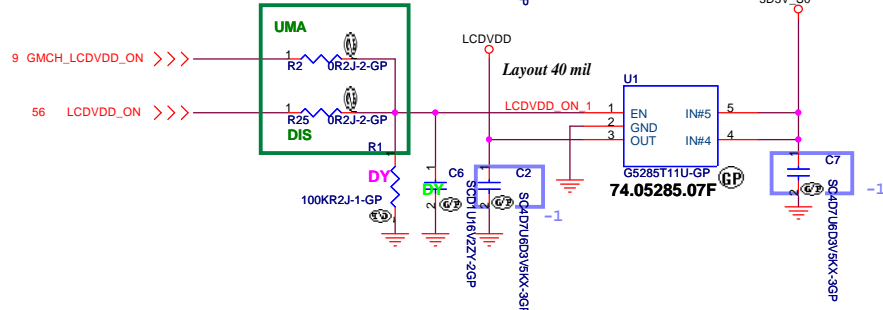
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
DDR DAMPING & TERMINATION		
Size	Document Number	Rev
A3	JV50-TR8	-1
Date:	Monday, October 26, 2009	Sheet 18 of 63

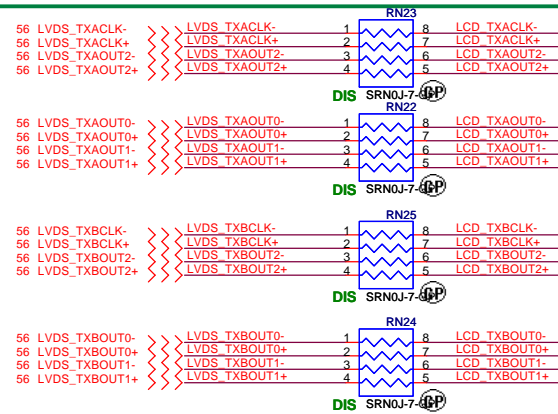
LCD/INVERTER/CCD CONN



for TR

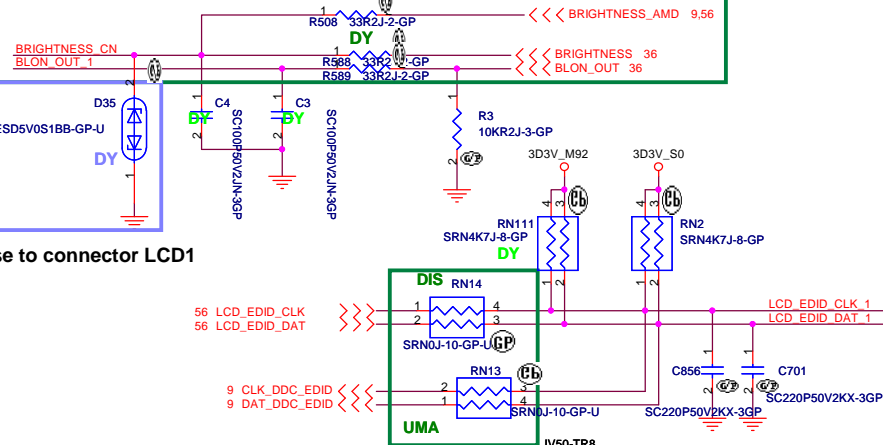
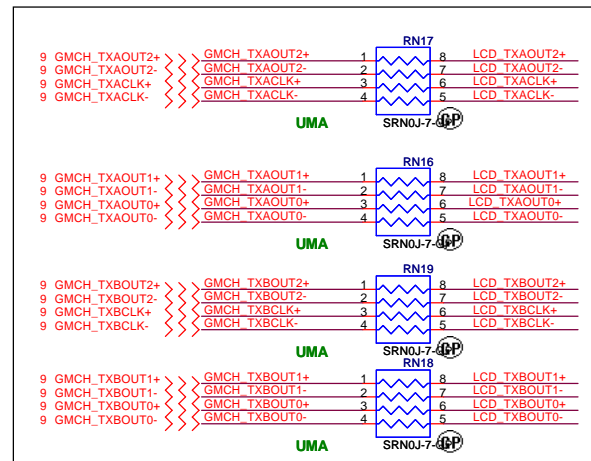


for TR

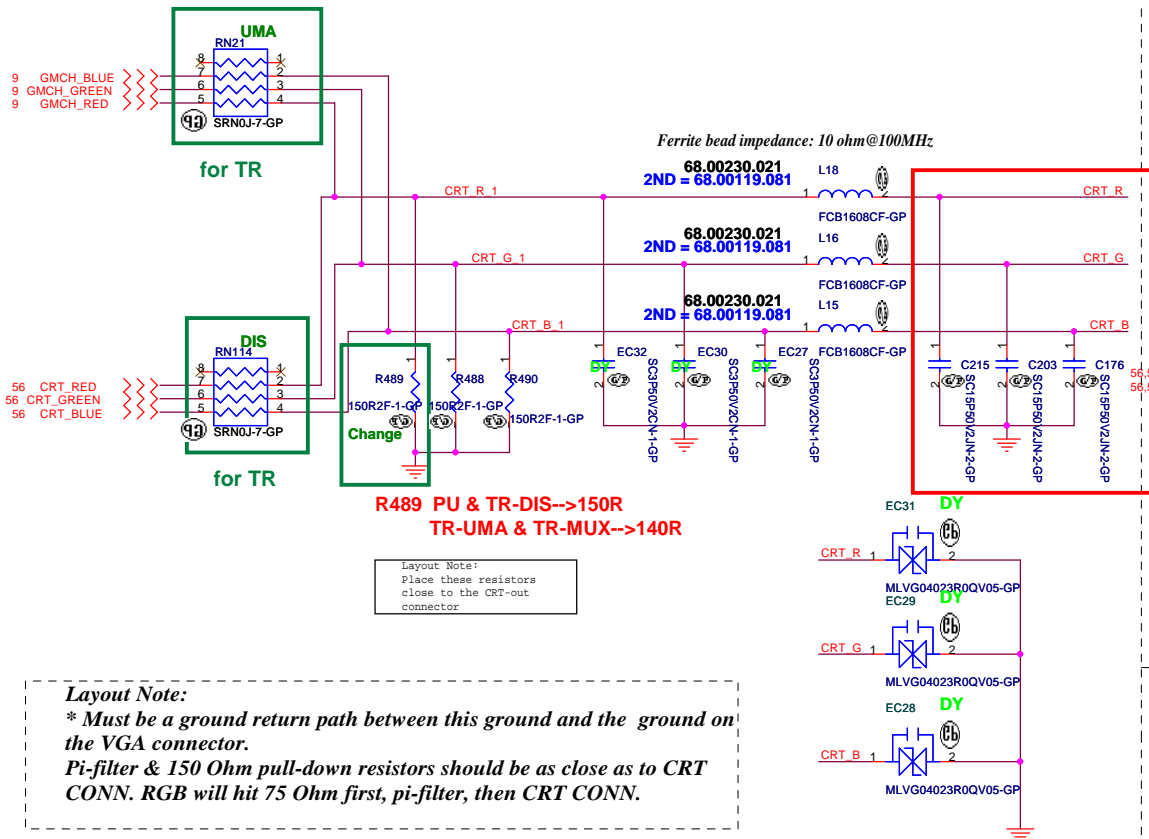


Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

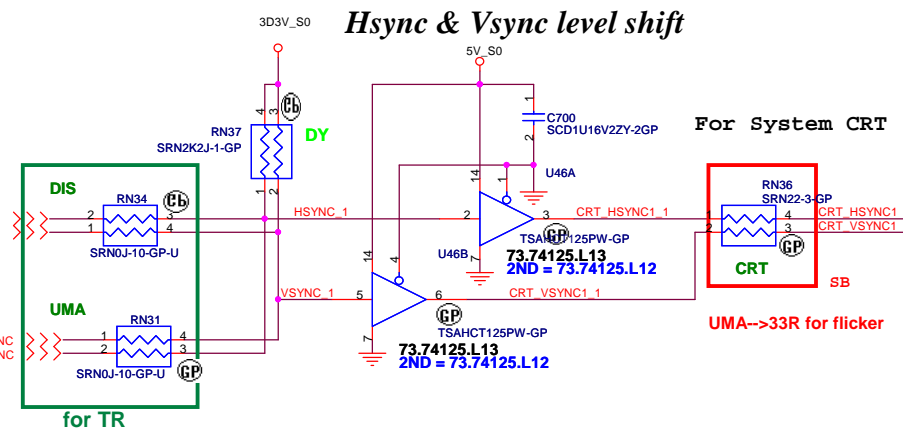
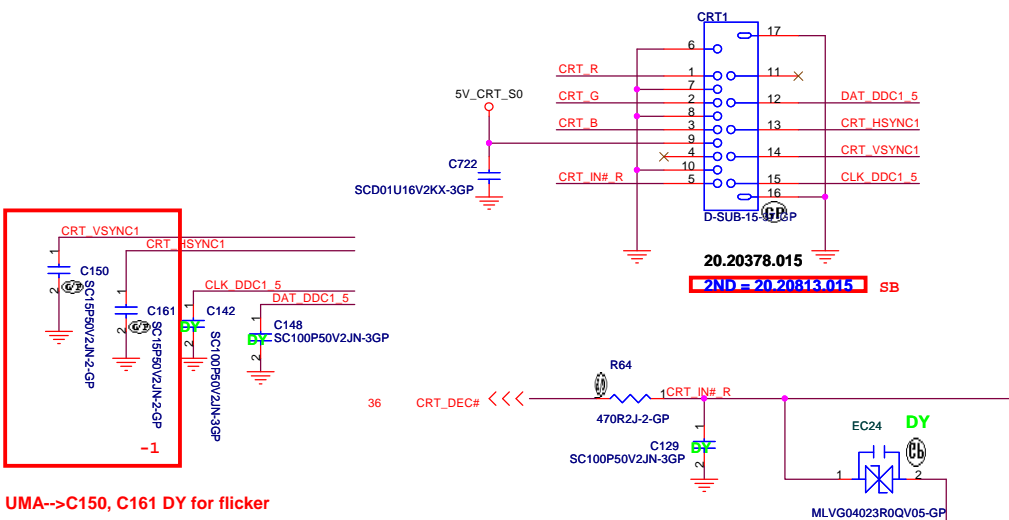
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND



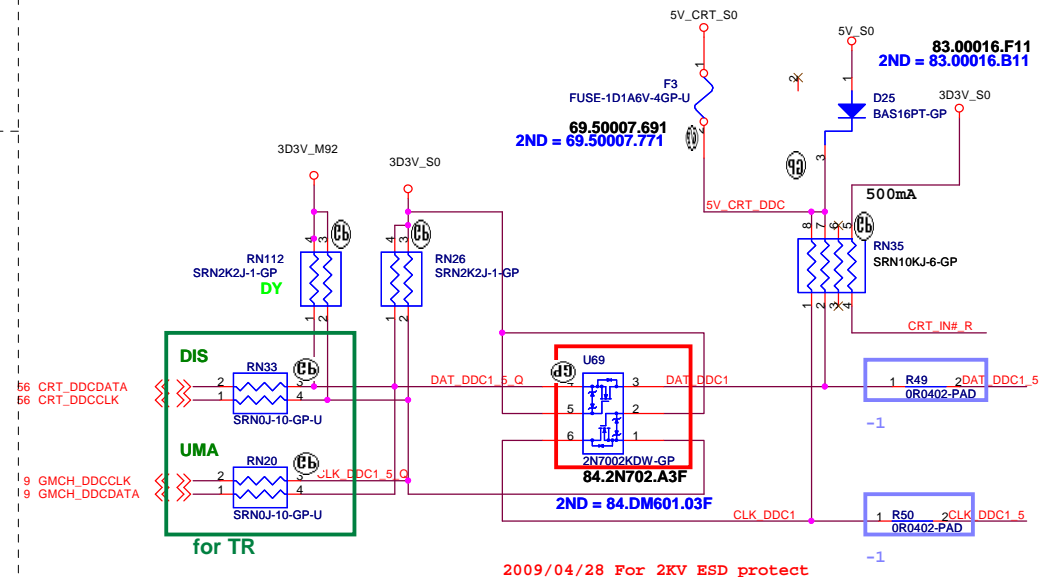
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.



CRT I/F & CONNECTOR



DDC_CLK & DATA level shift

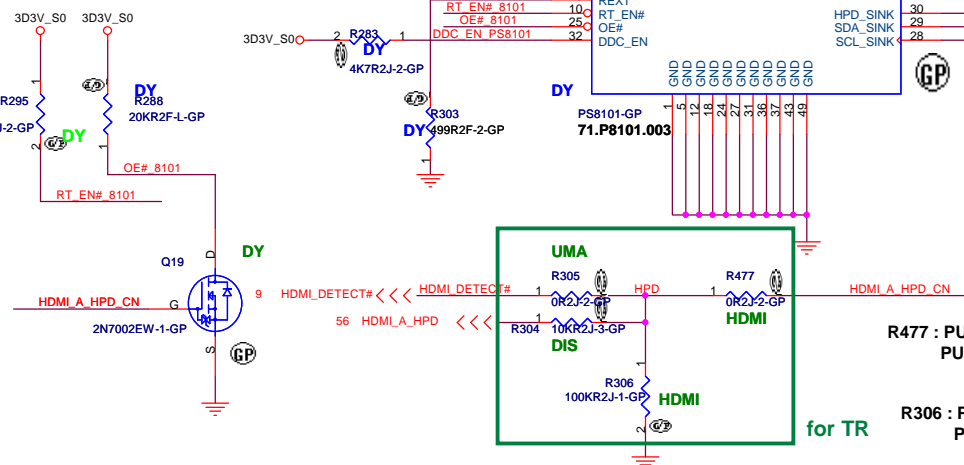
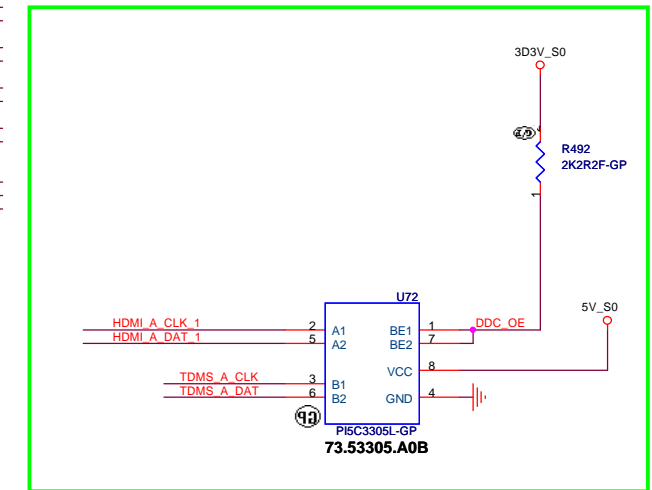
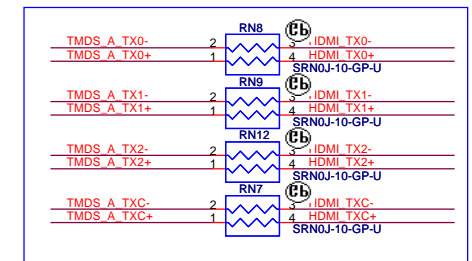
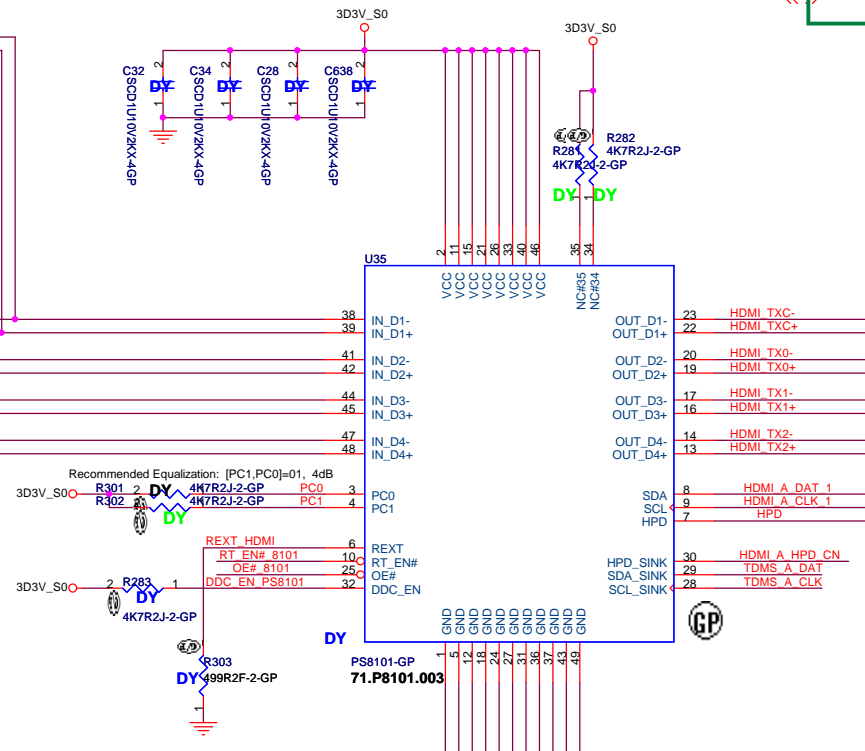
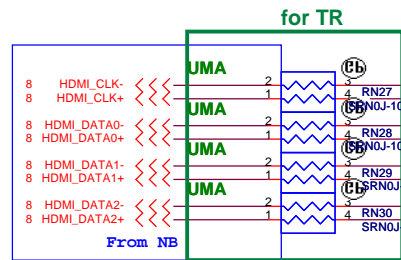
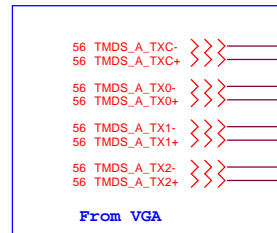
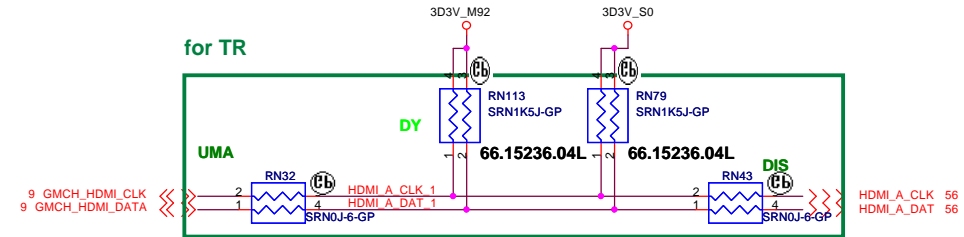


JV50-TR8

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CRT Connector		
Size	Document Number	Rev
	JV50-TR8	-1
Date: Monday, October 26, 2009	Sheet 20	of 63

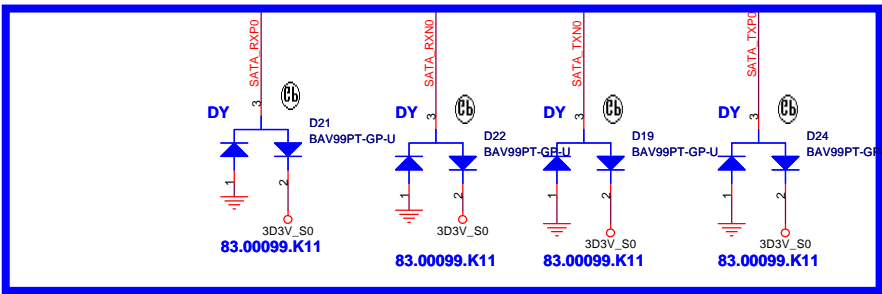
for TR



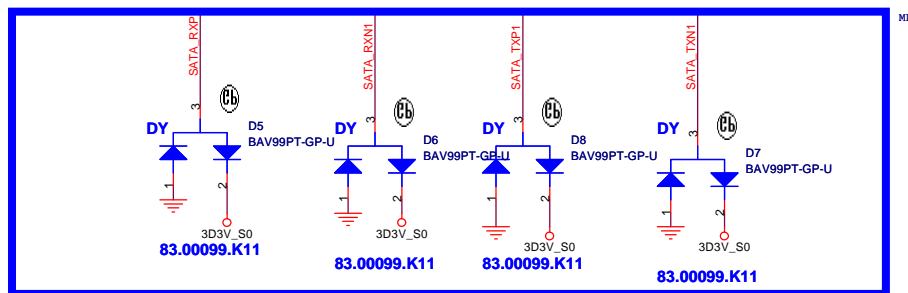
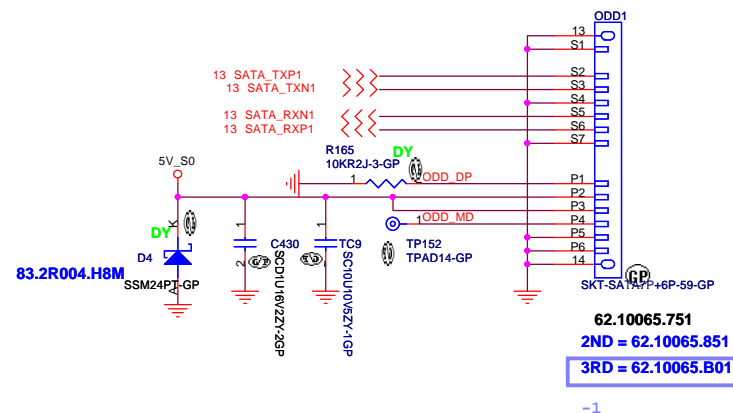
R477 : PU & TR-DIS-->0R
PU & TR-UMA & MUXLESS-->5.1K

R306 : PU & TR-DIS-->100K
PU & TR-UMA & MUXLESS-->10K

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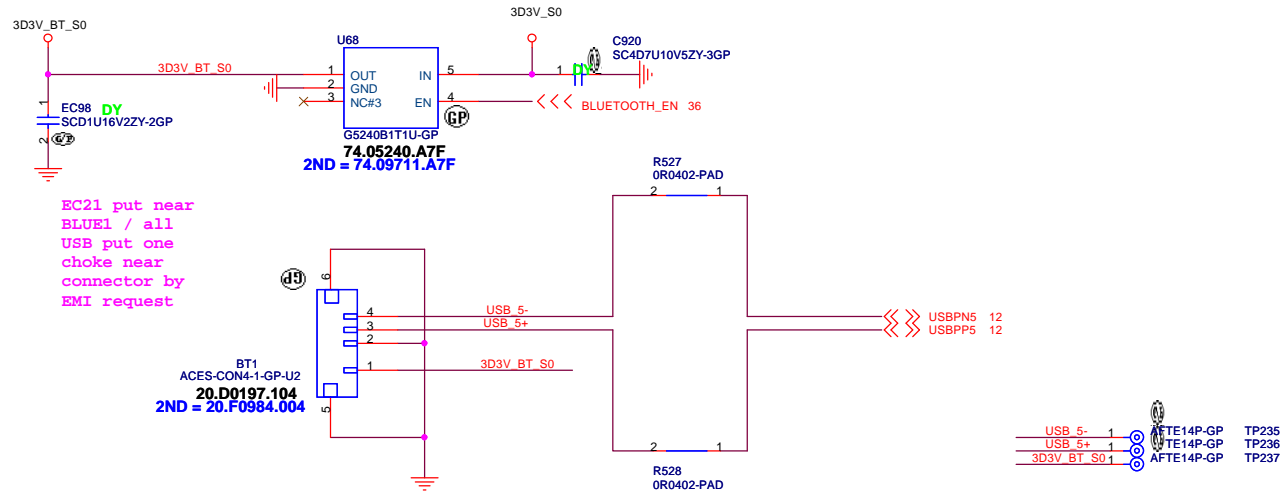


SATA ODD Connector



BLUETOOTH MODULE

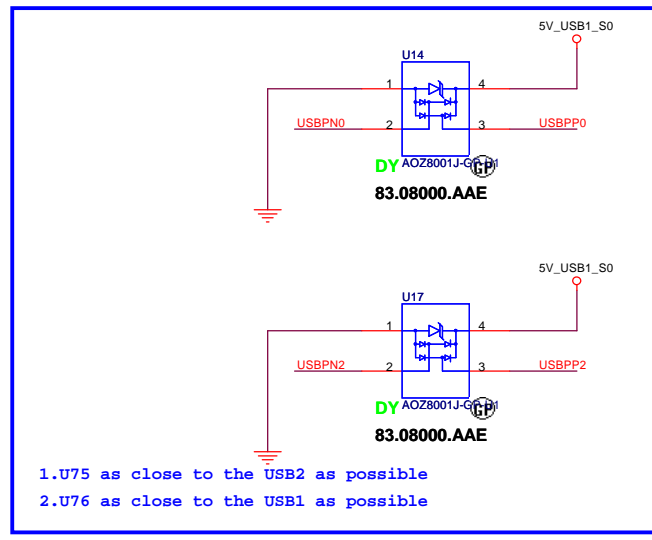
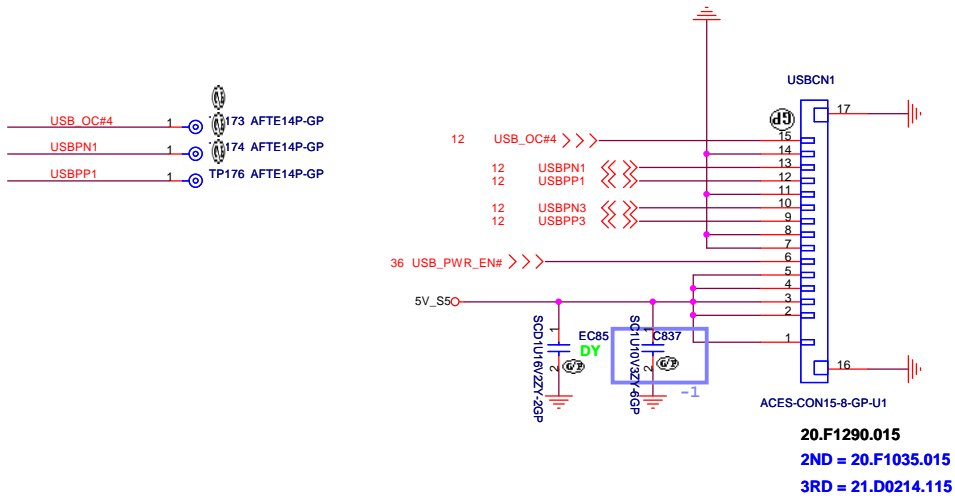
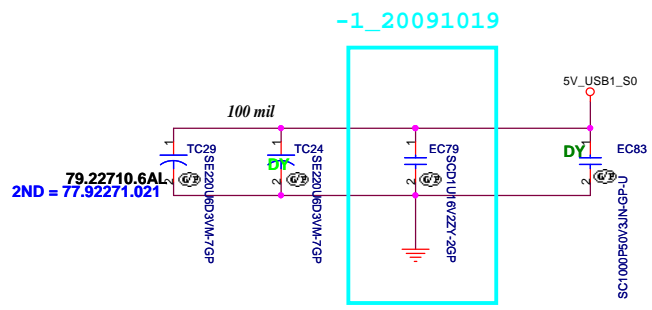
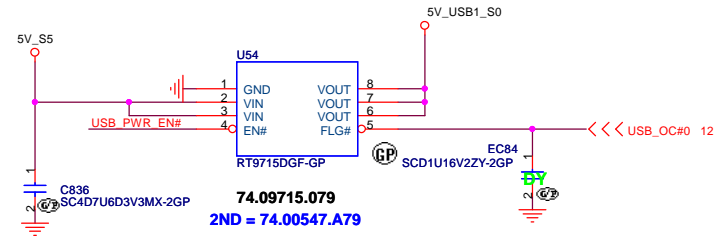
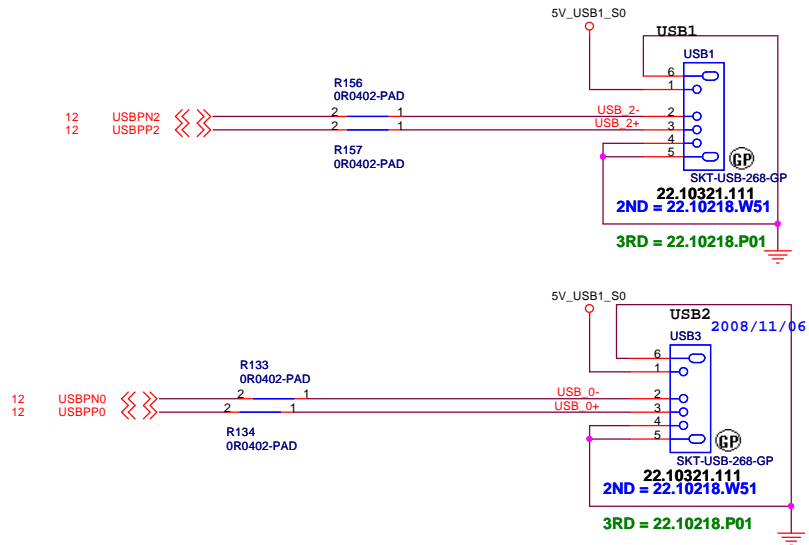
1.5A / High Active Voltage 2V



JV50-TR8

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Taipei Hsien 221, Taiwan, R.O.C.

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BLUETOOTH			
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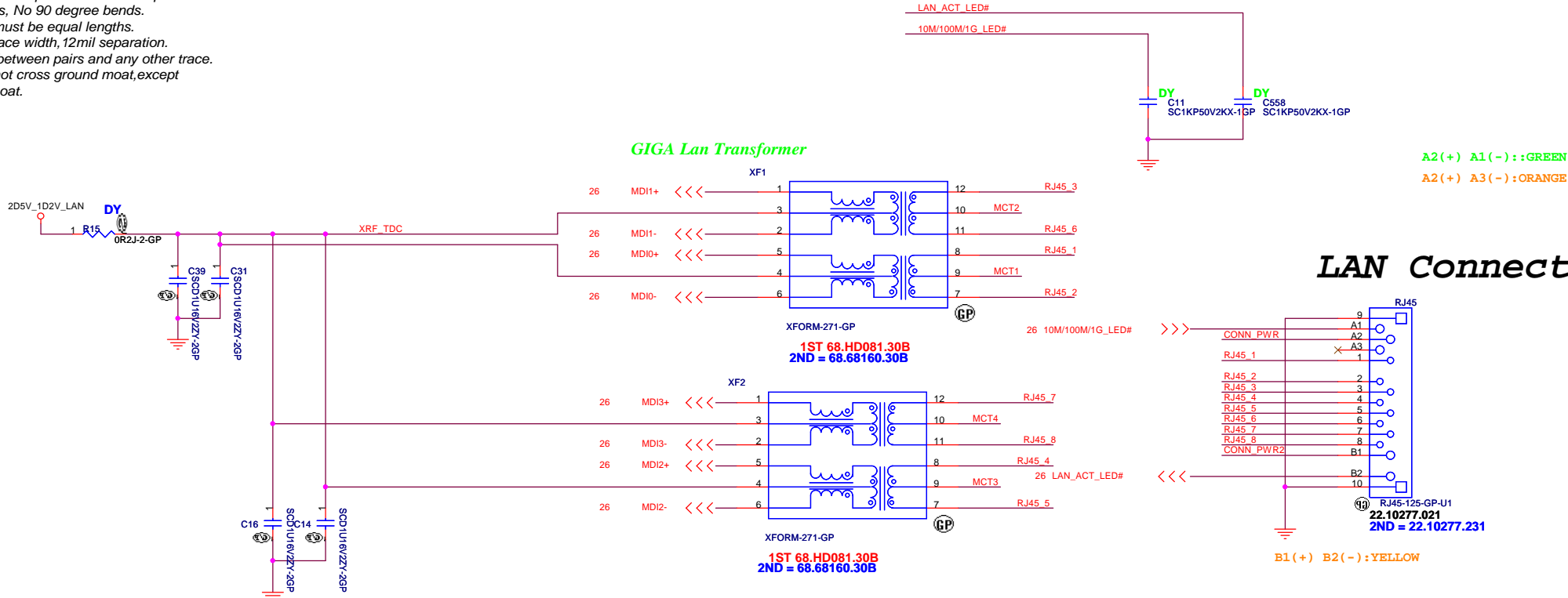


1.U75 as close to the USB2 as possible
2.U76 as close to the USB1 as possible

JV50-TR8

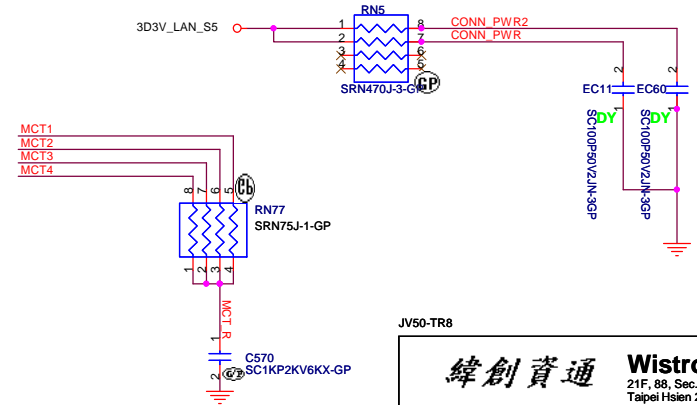
LAN Connector

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

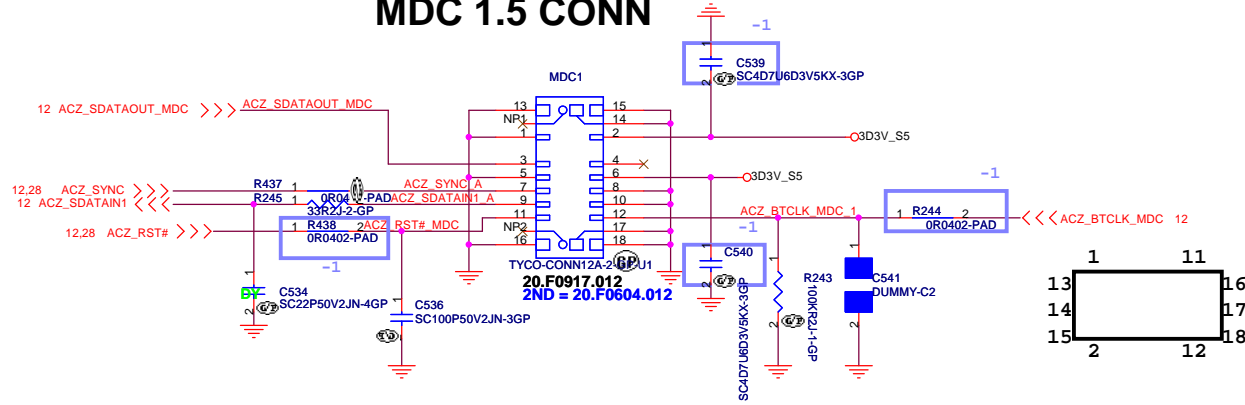


LAN Connector

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

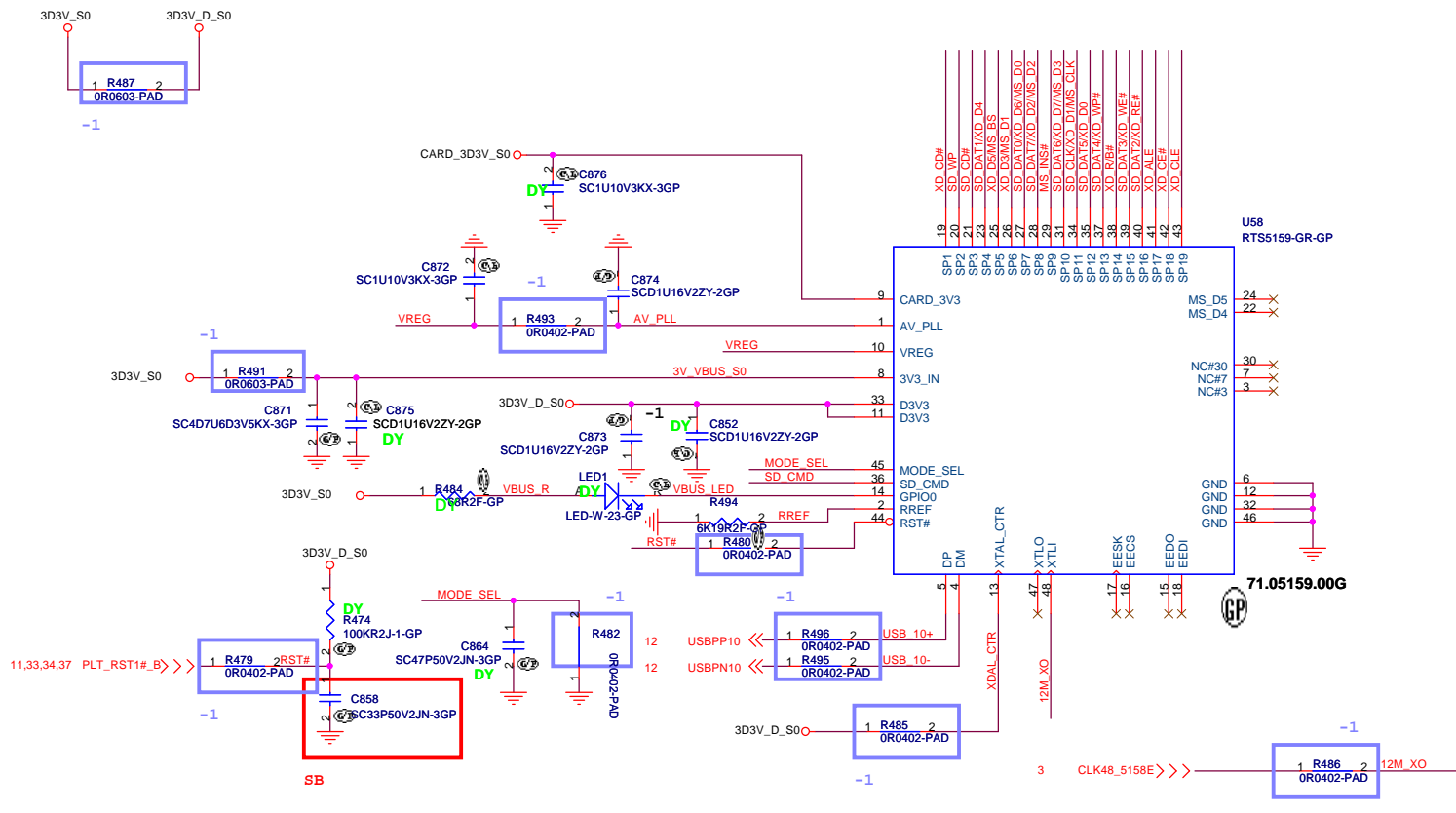


MDC 1.5 CONN

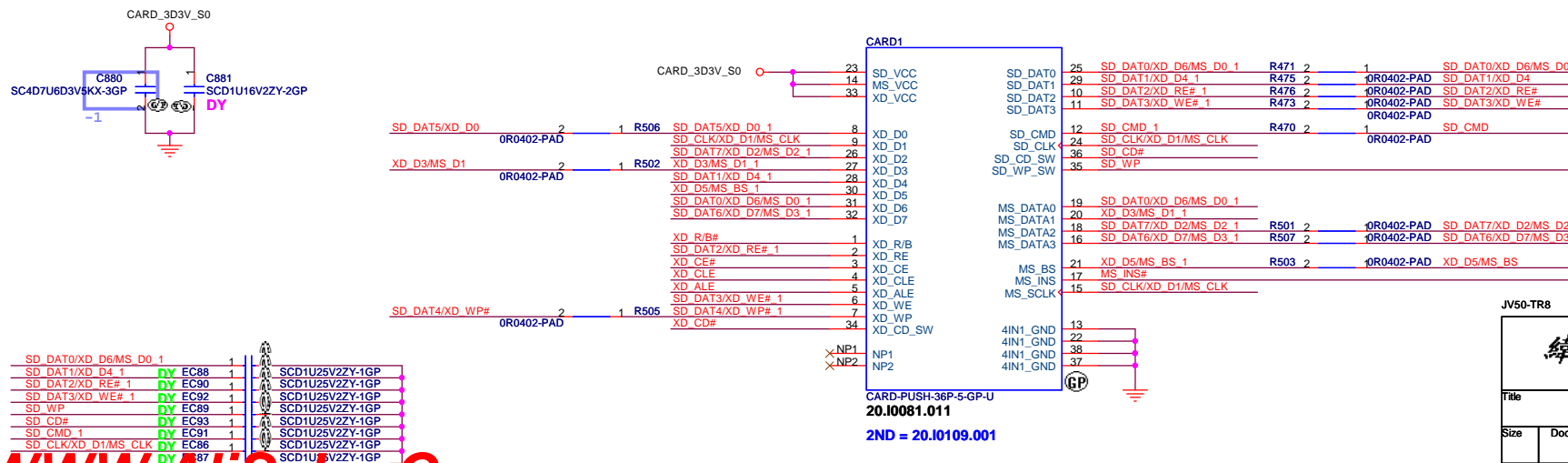


JV50-TR8

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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5 IN 1 CARD-READER (SD/MMC/MS/MS PRO/XD)



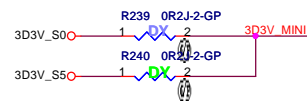
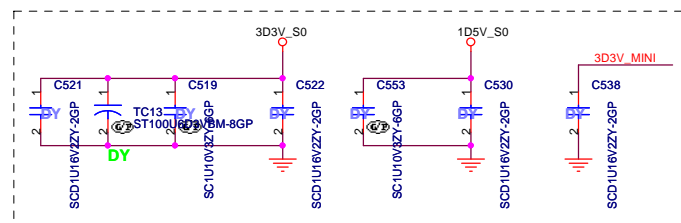
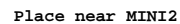
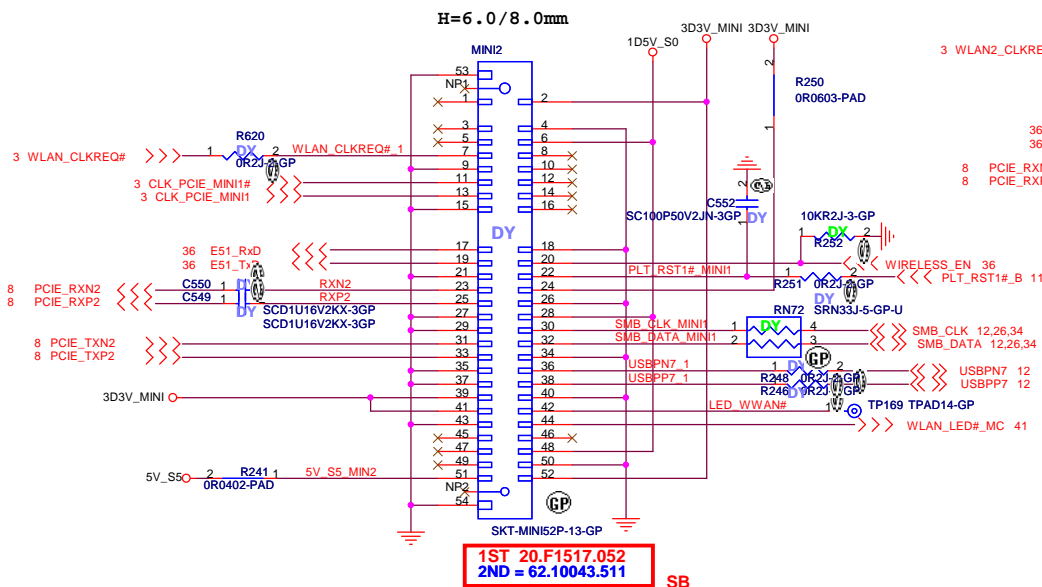
JV50-TR8

緯創資通

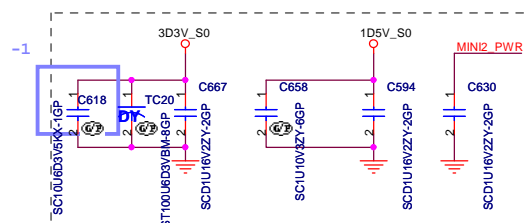
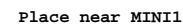
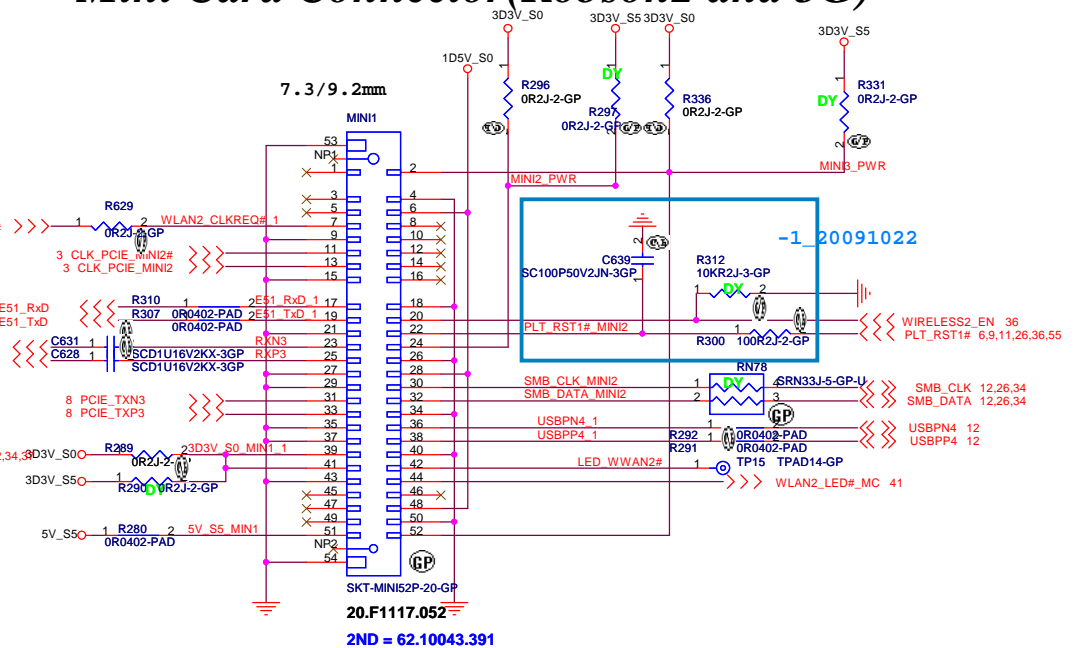
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

CARDREADER- RTS5159			
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Mini Card Connector(WLAN)



Mini Card Connector(Robson2 and 3G)



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緯創資通

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Title

MINI CARD

Size	Document Number
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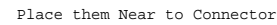
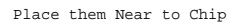
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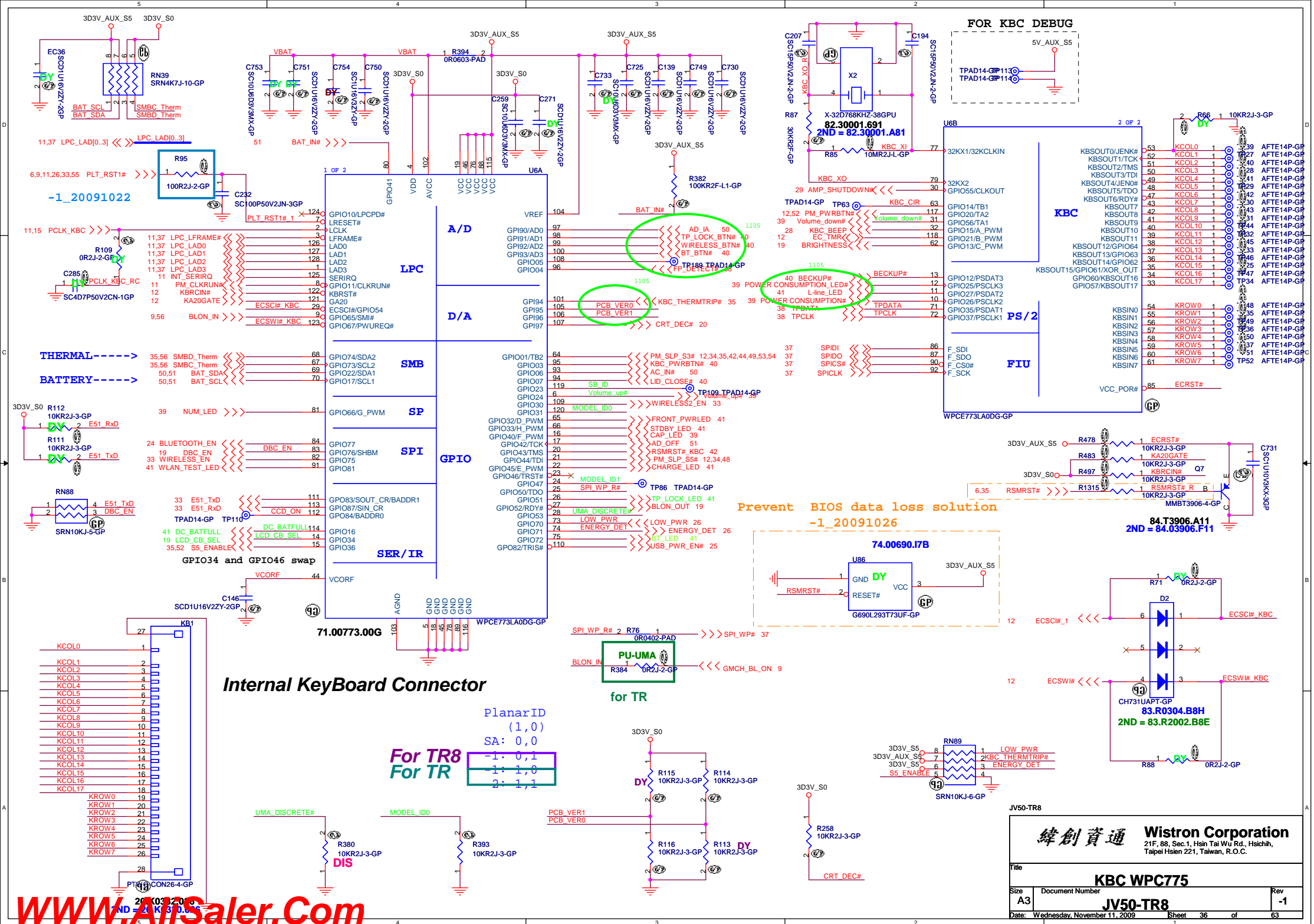
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

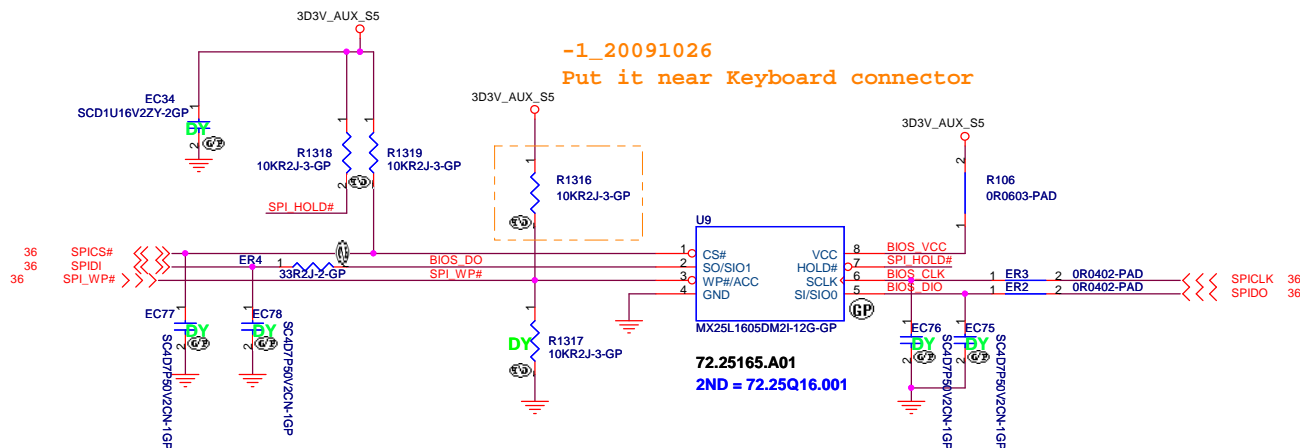
NEW CARD

JV50-TR8

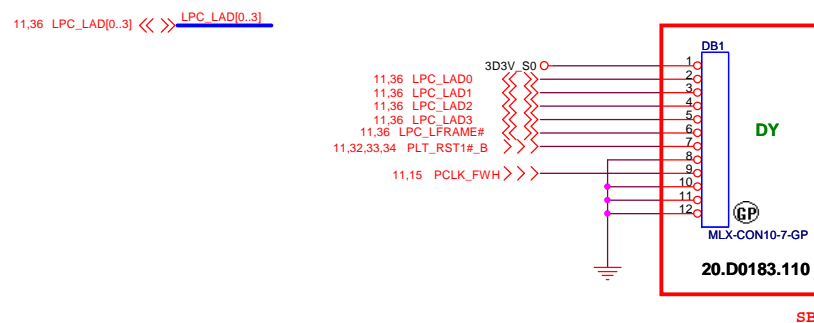
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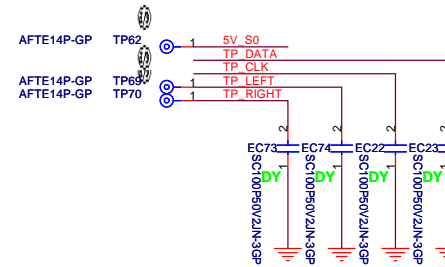
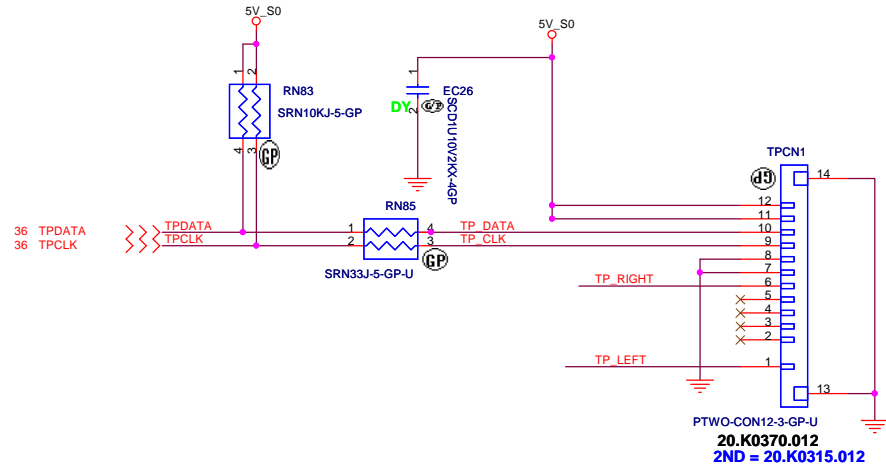


**16M Bits
SPI FLASH ROM
GOLDEN FINGER FOR DEBUG BOARD**

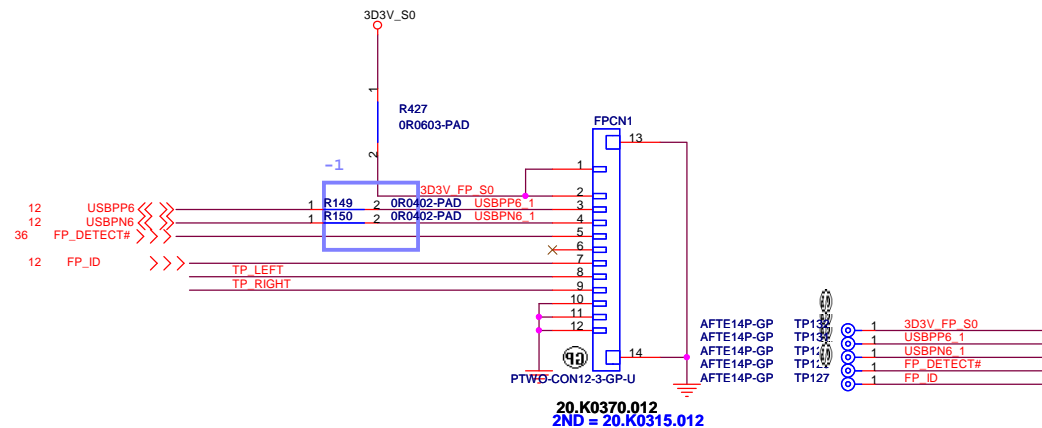


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TOUCH PAD



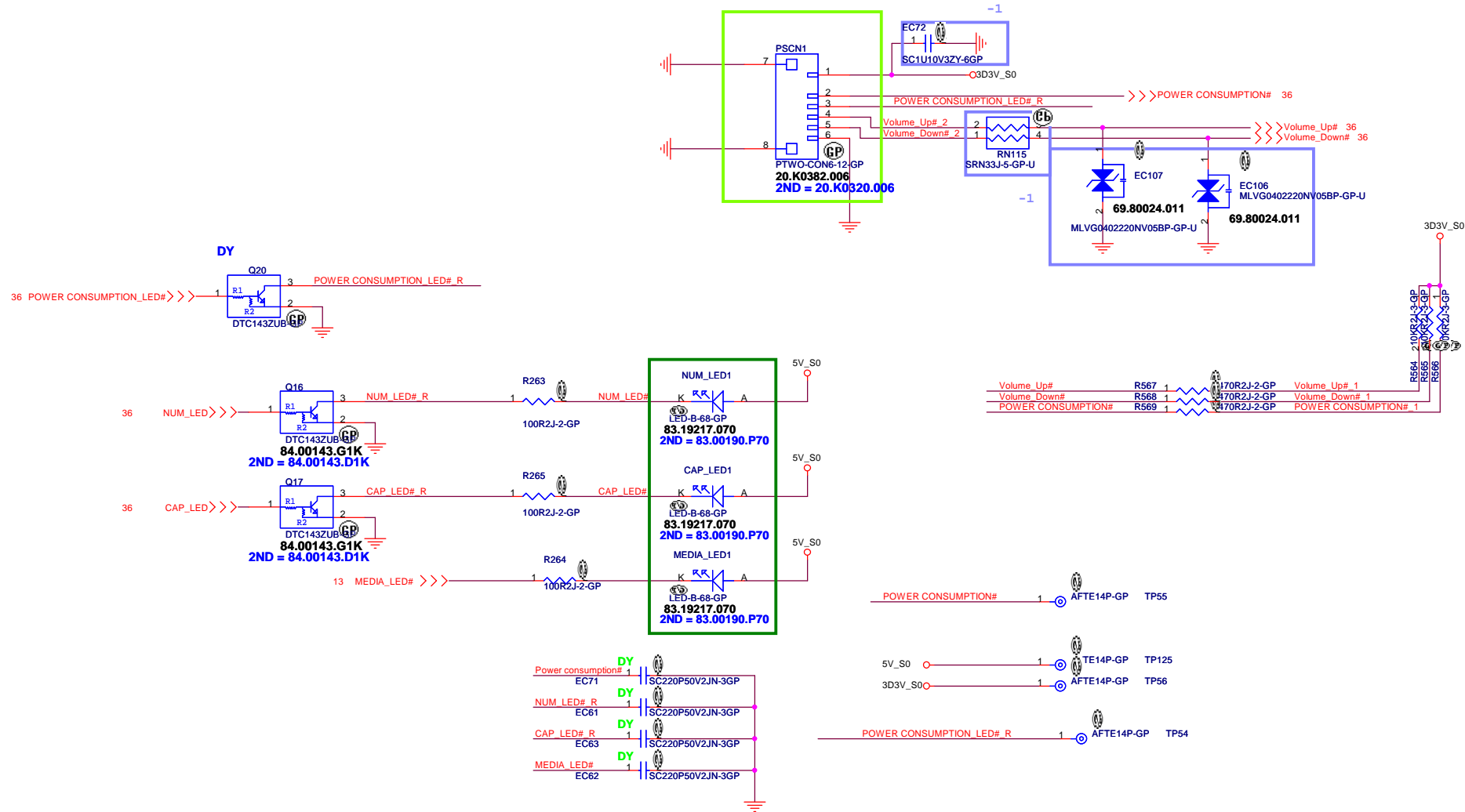
Finger printer



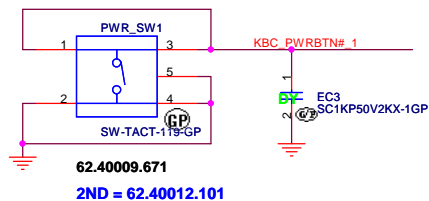
JV50-TR8

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

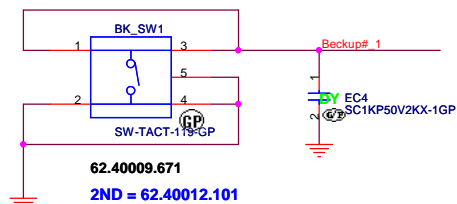
Title		
Touch PAD/Finger printer		
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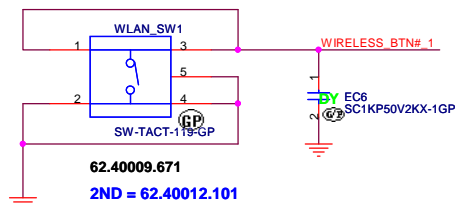
Power Button



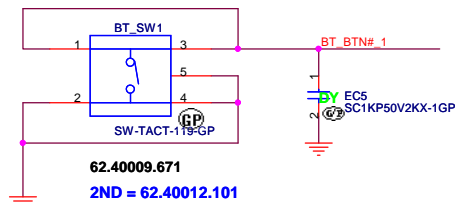
Beckup Button



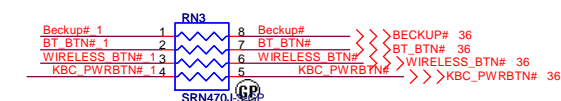
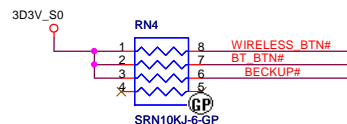
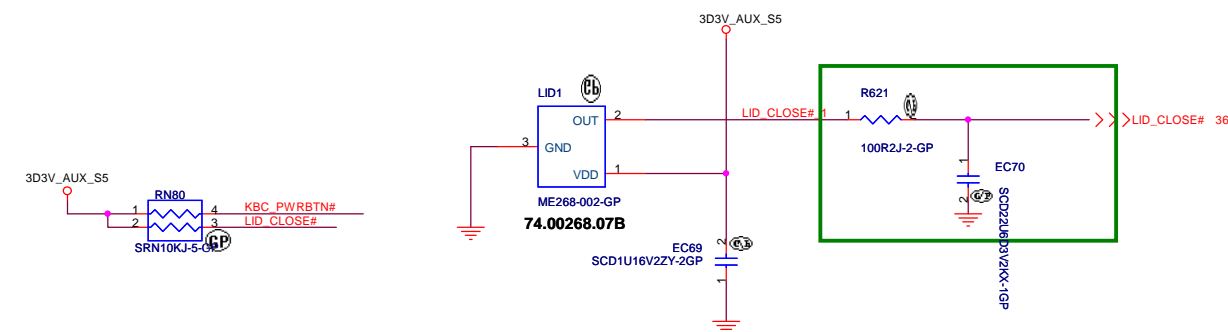
WIRELESS Button



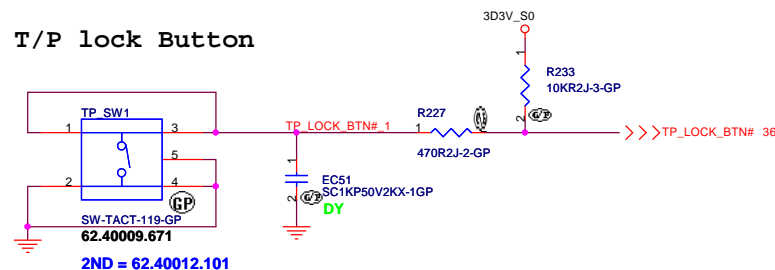
BT/3G Button



Cover Up Switch

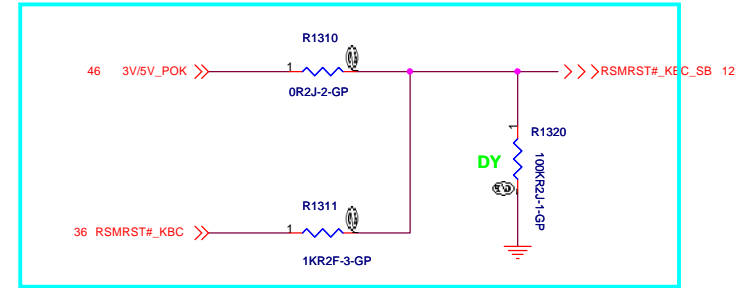
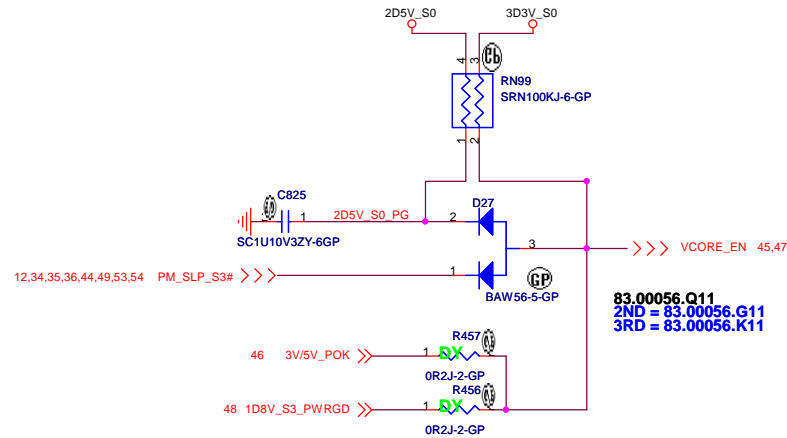


T/P lock Button



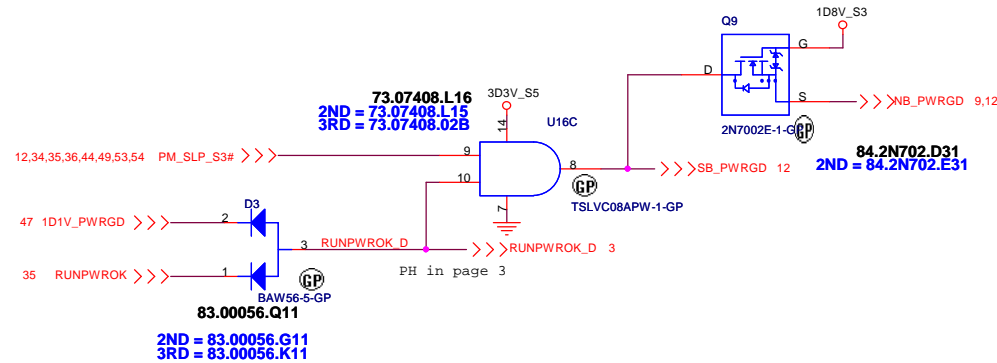
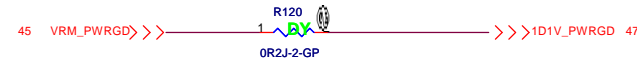
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			SWITCH
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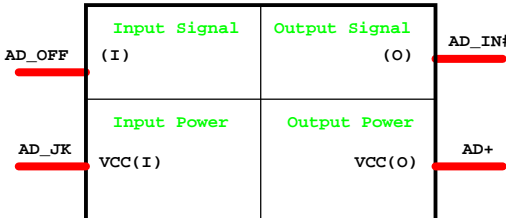


JV50-TR8

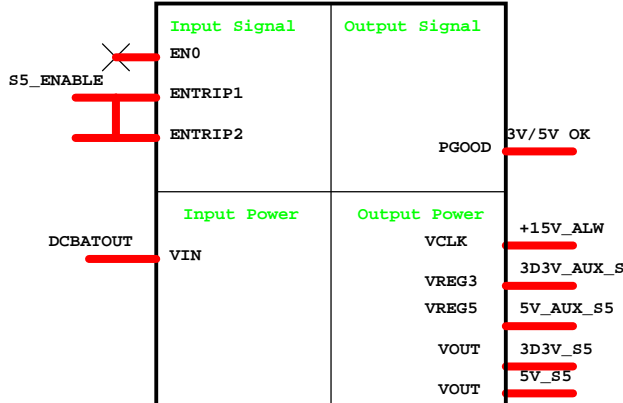
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
POWER ON LOGIC		
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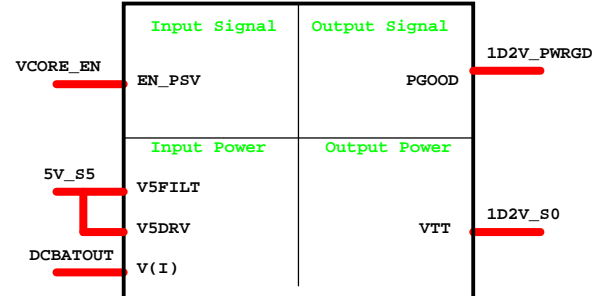
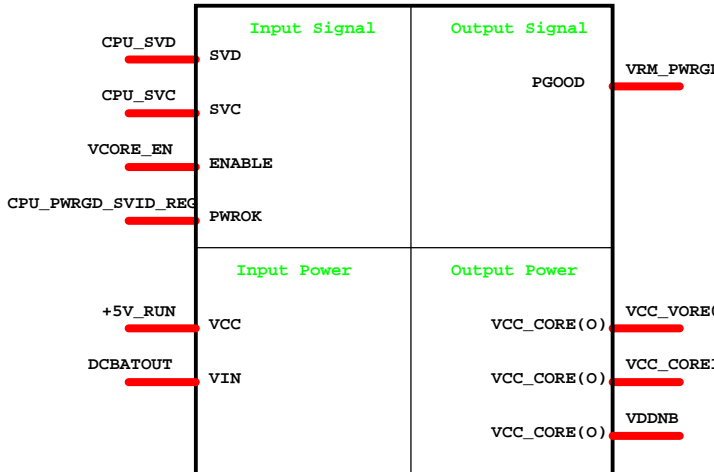
Adapter



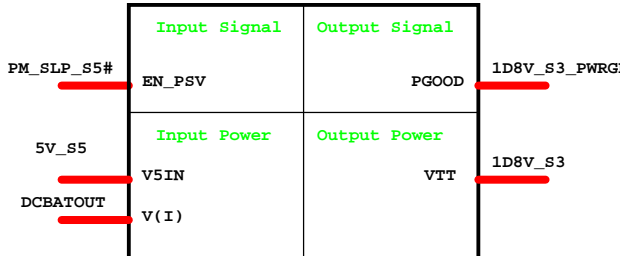
DCDC 5V/3D3V(RT8205A)



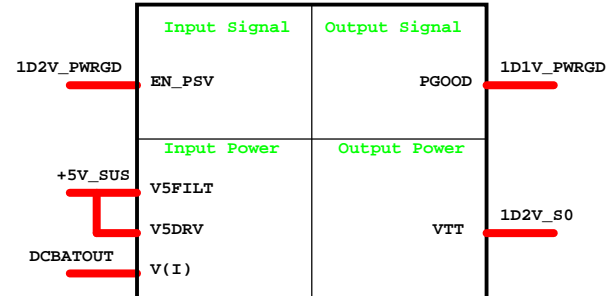
DCDC 1D2V(TPS51124)

CPU_CORE
ISL6265HRTZ

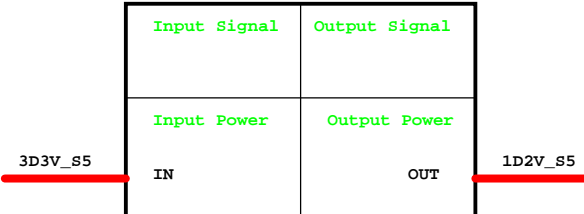
DCDC 1D8V(RT8209B)



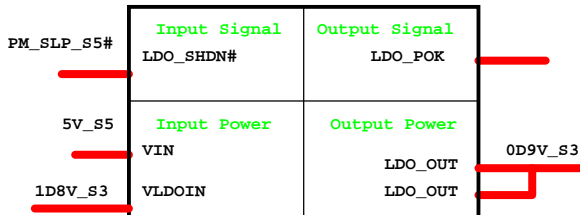
DCDC 1D1V(TPS51124)



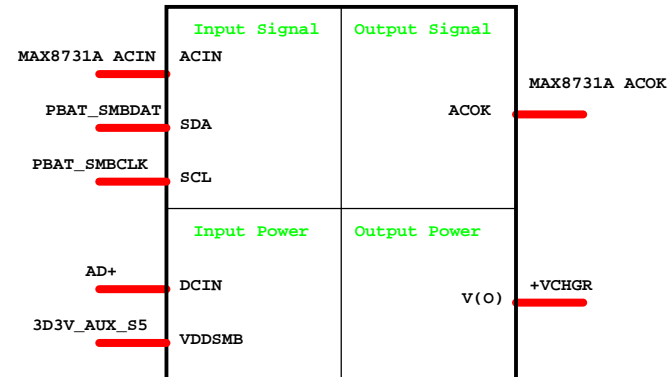
1D2V LDO G9161



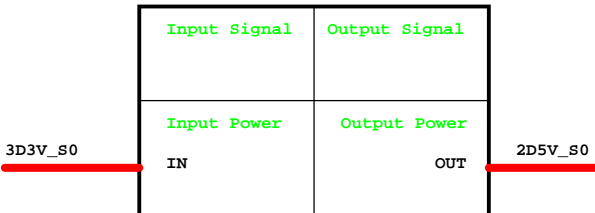
0D9V LDO RT9026



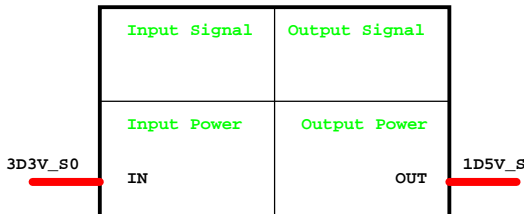
CHARGER MAX8731

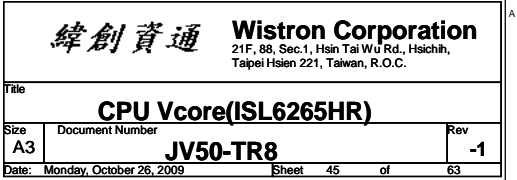


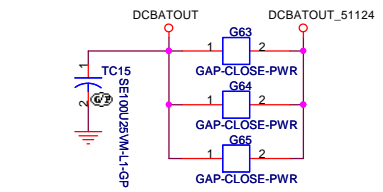
2D5V LDO R9161



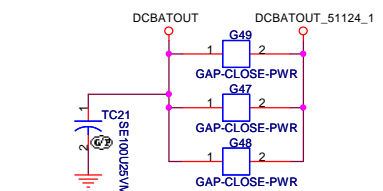
1D5V LDO G9571





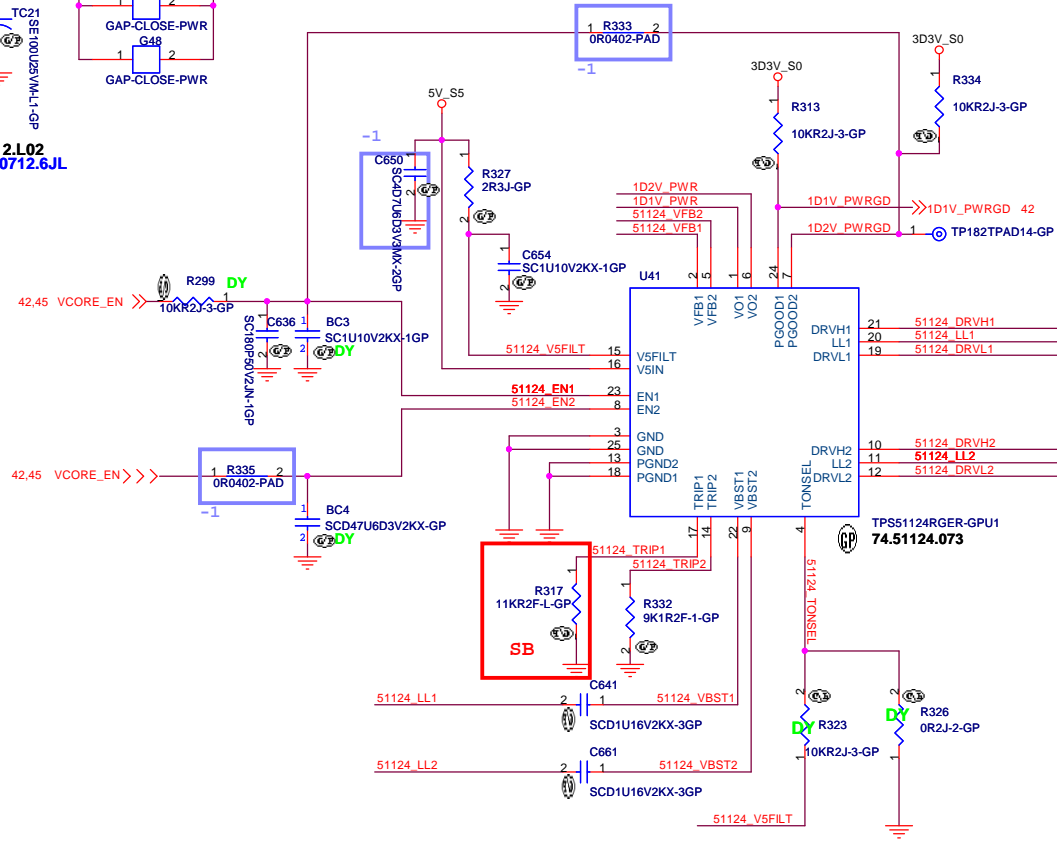


79.10712.L02
2ND = 79.10712.6JL



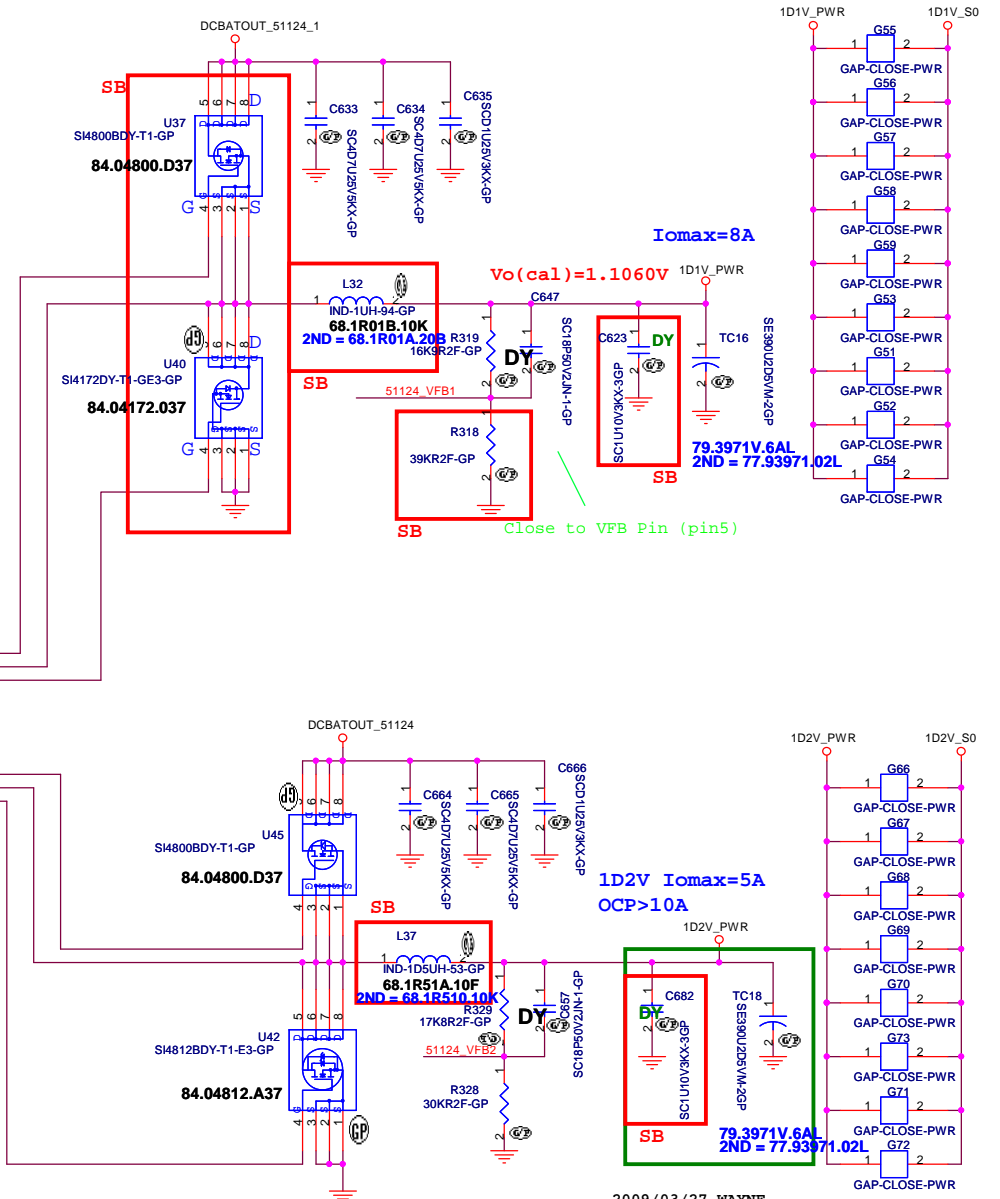
79.10712.L02
2ND = 79.10712.6JL

$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$
 $I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out}) / V_{in}))$



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

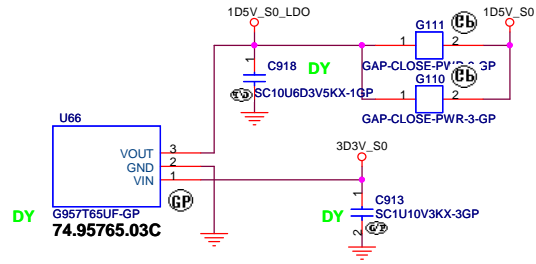
$V_{out} = 0.758V * (R1+R2)/R2$ --> PWM mode
 $V_{out} = 0.764V * (R1+R2)/R2$ --> Skip Mode



2009/03/27 WAYNE
C682 change to 1u10v for ESL

G957

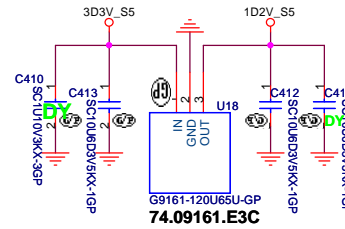
1D5V_S0
Iomax=1A



For MINI Card.NEW Card power SW

G9161

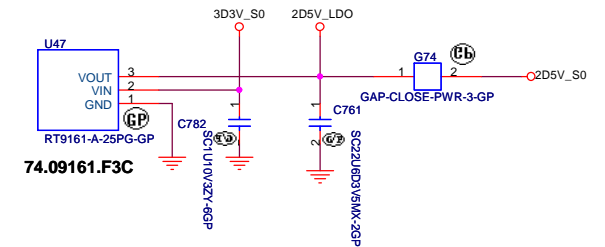
1D2V_S5
Iomax=400mA



Place near to SB710

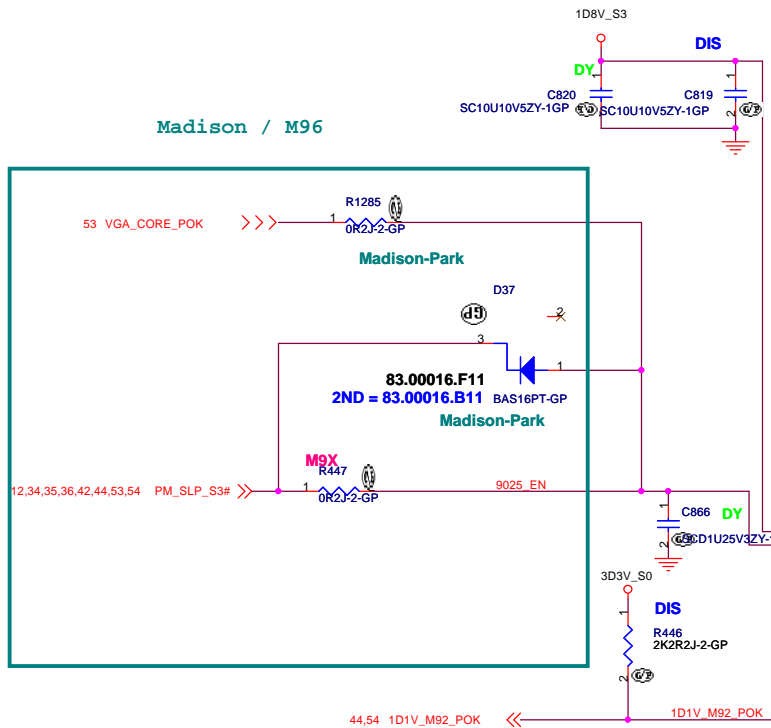
RT9161A

2D5V
Iomax=0.2A



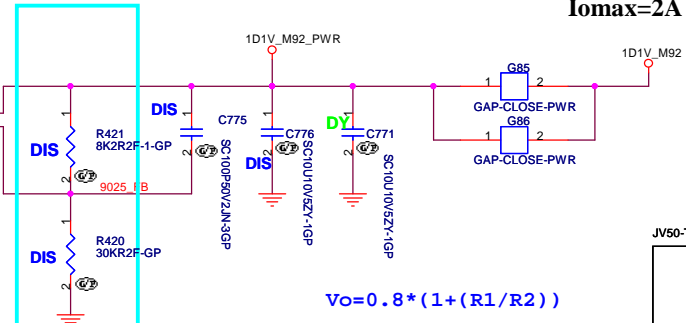
Place near to CPU

Madison / M96



Now set to 1V for Madison

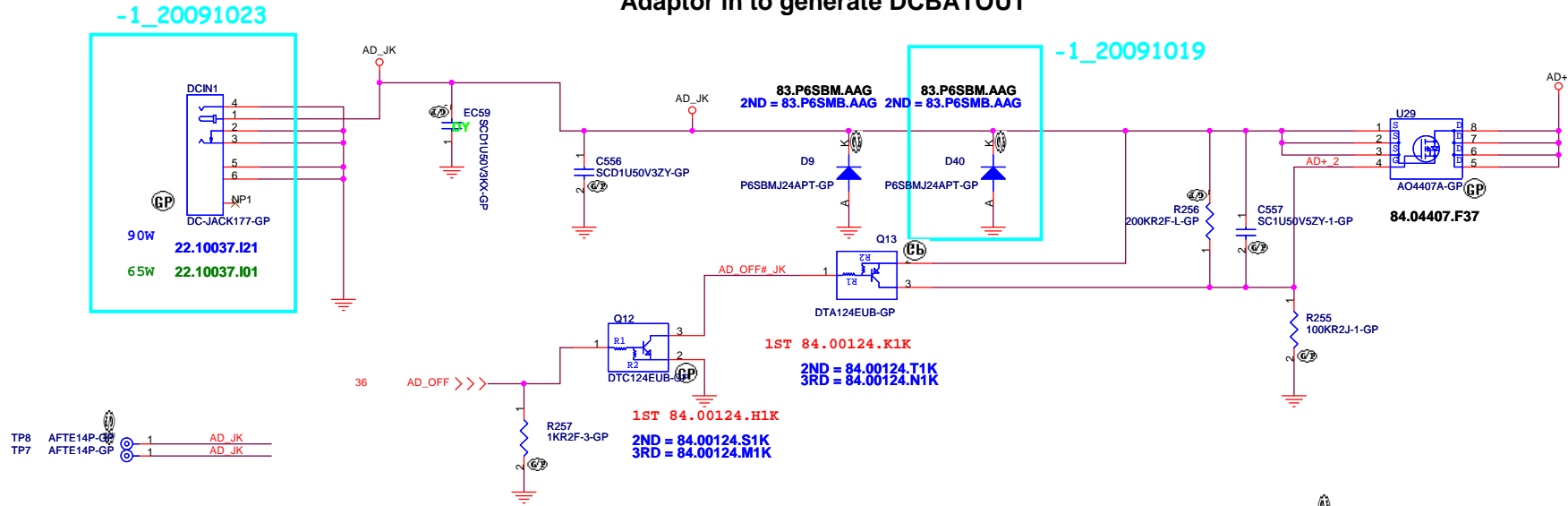
VO	R421	P/N
1D1V	11K5	64.11525.6DL
1V	8K2	64.82015.6DL



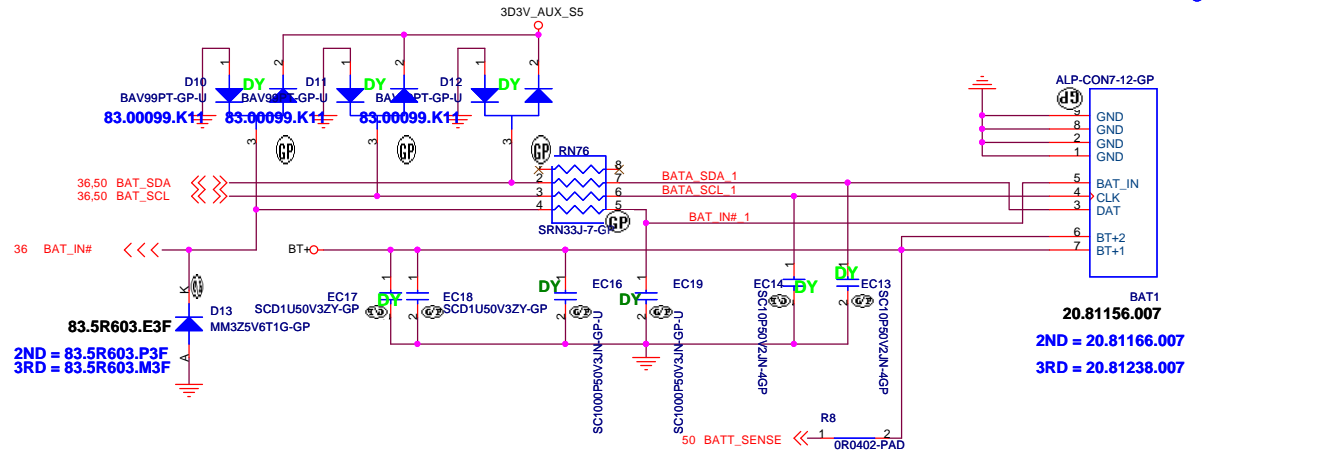
$$Vo = 0.8 * (1 + (R1/R2))$$

JV50-TR8

Adaptor in to generate DCBATOUT



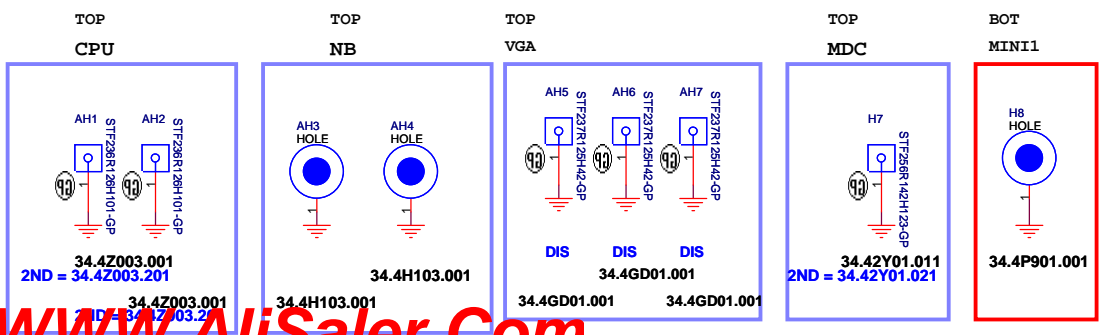
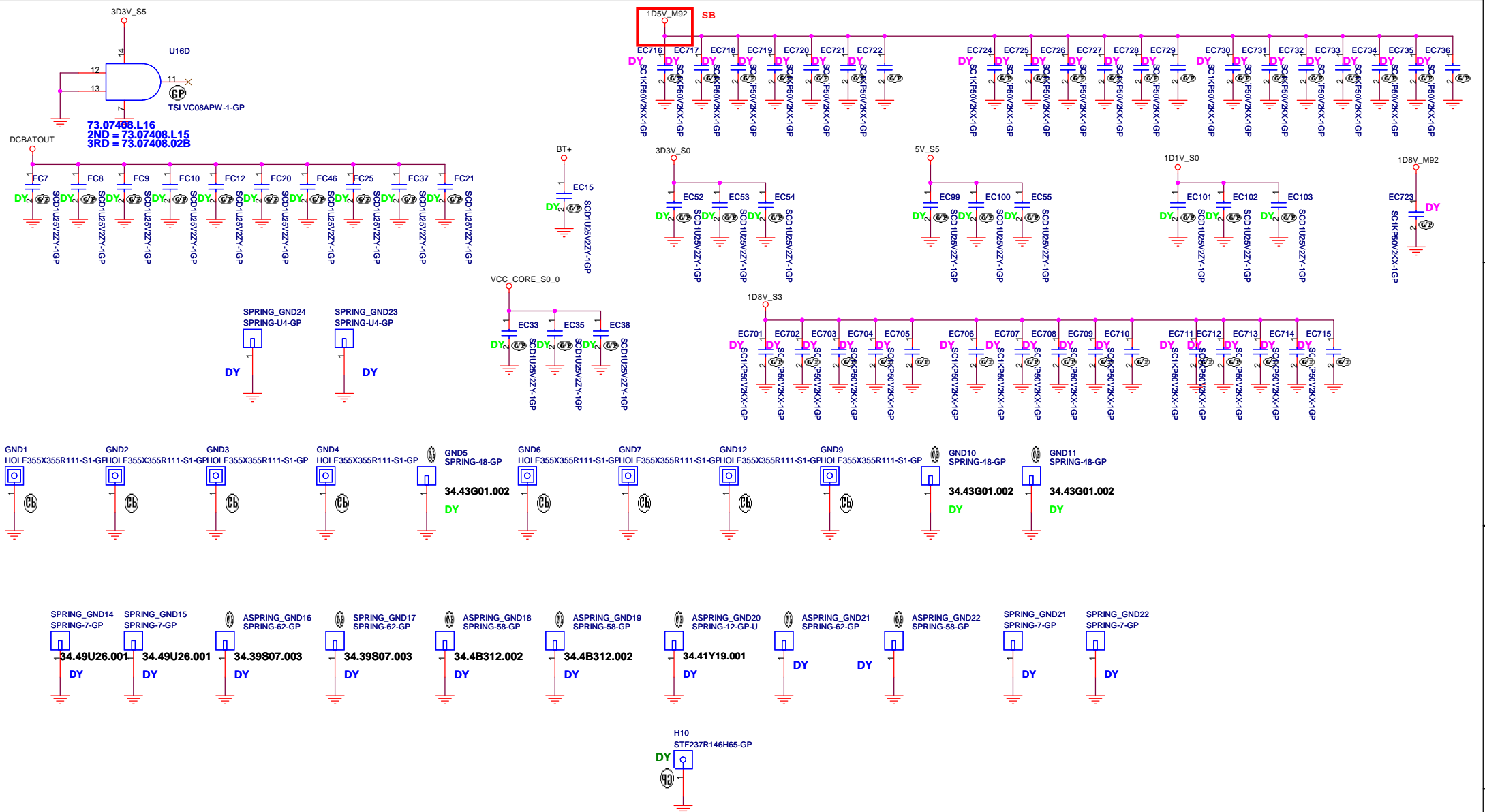
BATTERY CONNECTOR



緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

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Check test point

3D3V_S0	TP233	TPAD14-GP
3D3V_AUX_S5	TP232	TPAD14-GP
3D3V_S5	TP231	TPAD14-GP
5V_S5	TP230	TPAD14-GP
12,36 PM_PWRBTN#	TP229	TPAD14-GP
6,11 CPU_PWRGD	TP228	TPAD14-GP
35,36 SS_ENABLE	TP227	TPAD14-GP
6,11 CPU_LDT_RST#	TP226	TPAD14-GP

Test Point放在Dimm Door打開可量測處

JV50-TR8

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

Title

EMI/Spring/Boss

Size

Document Number

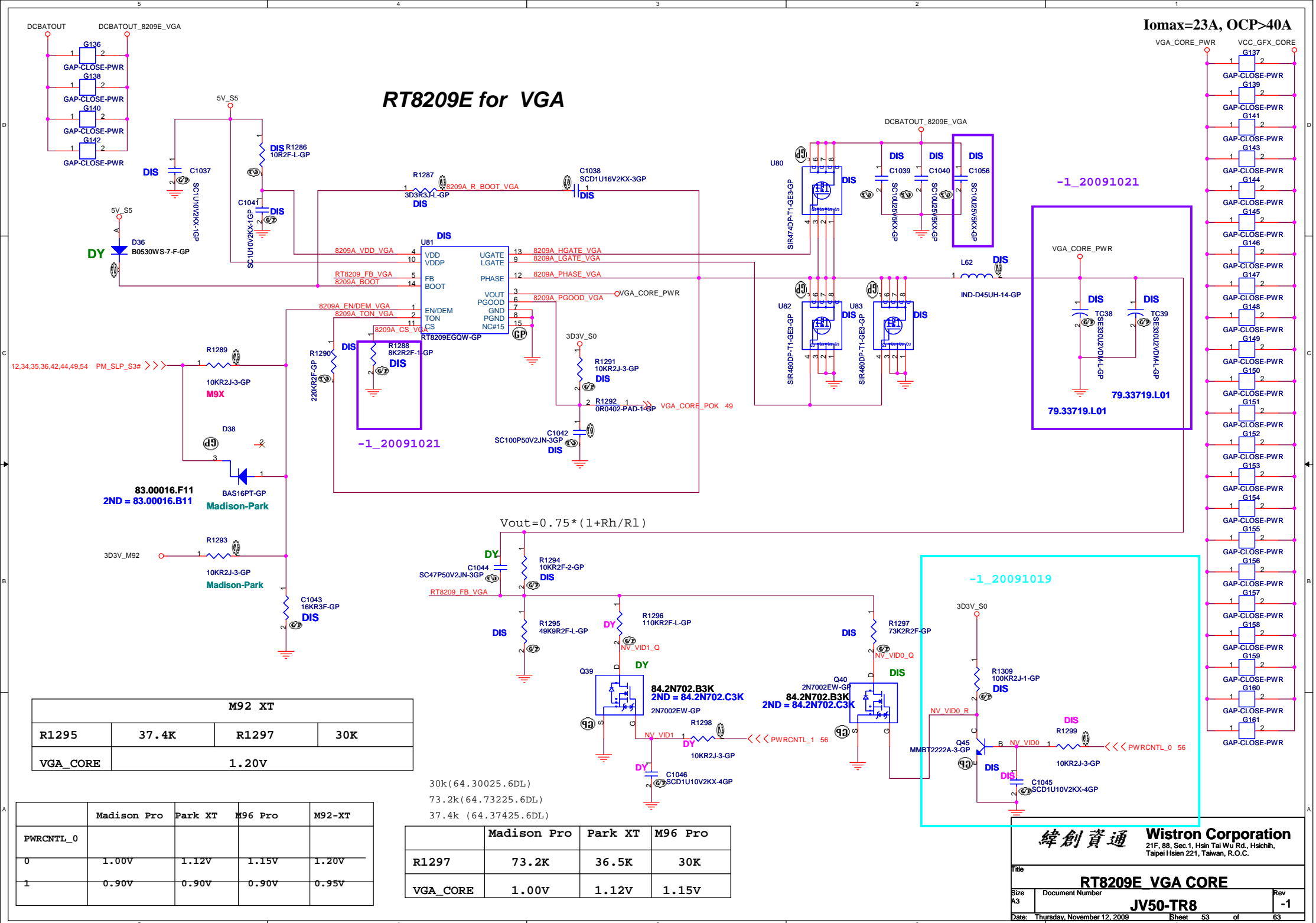
Rev

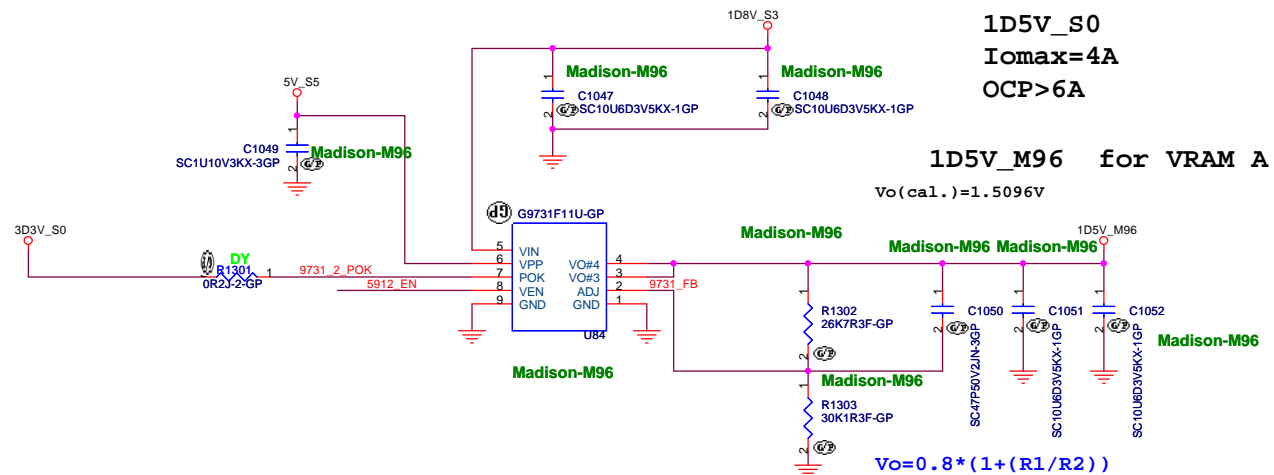
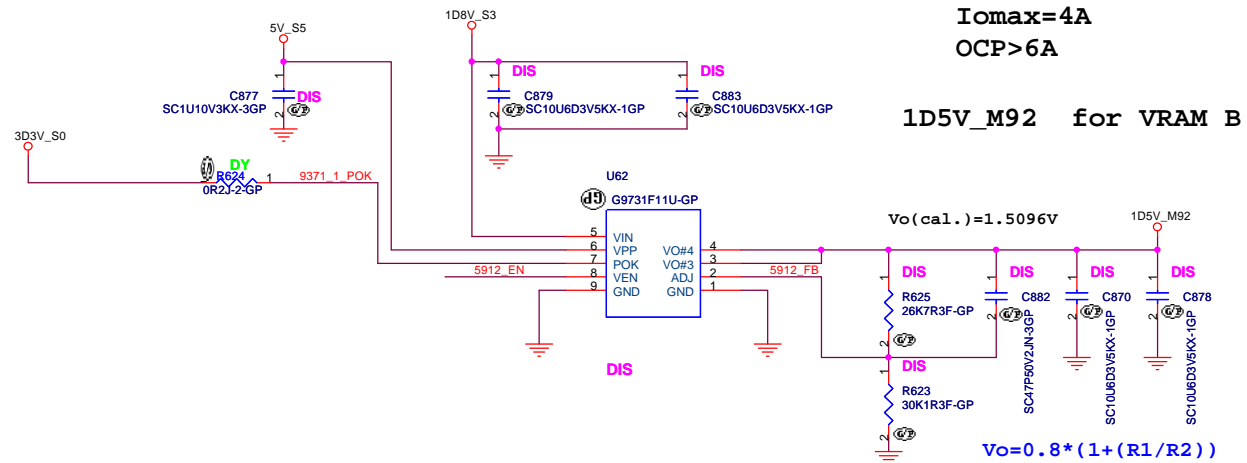
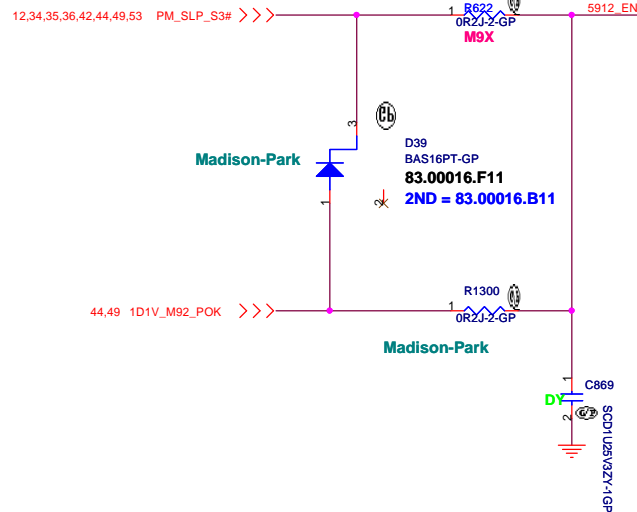
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		G9731 1D5V VRAM POWER	
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for TR

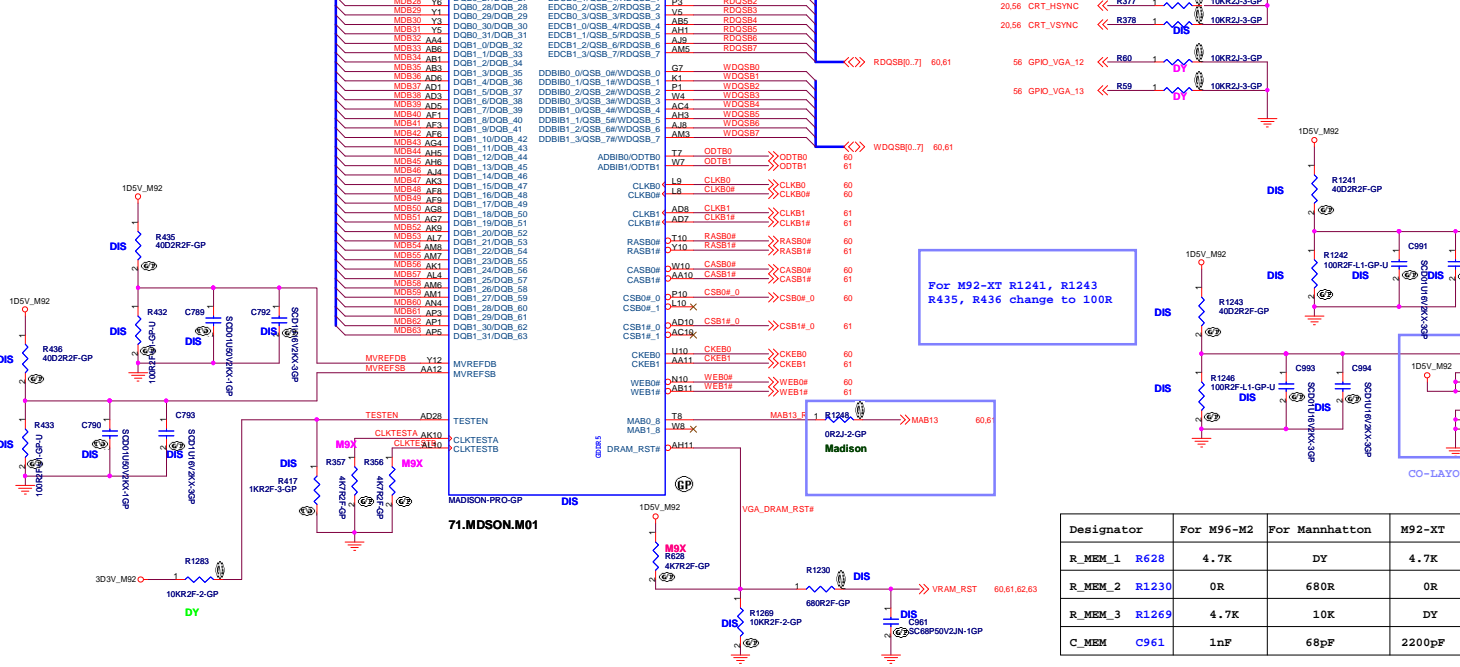


Title				Madison IO			
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For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

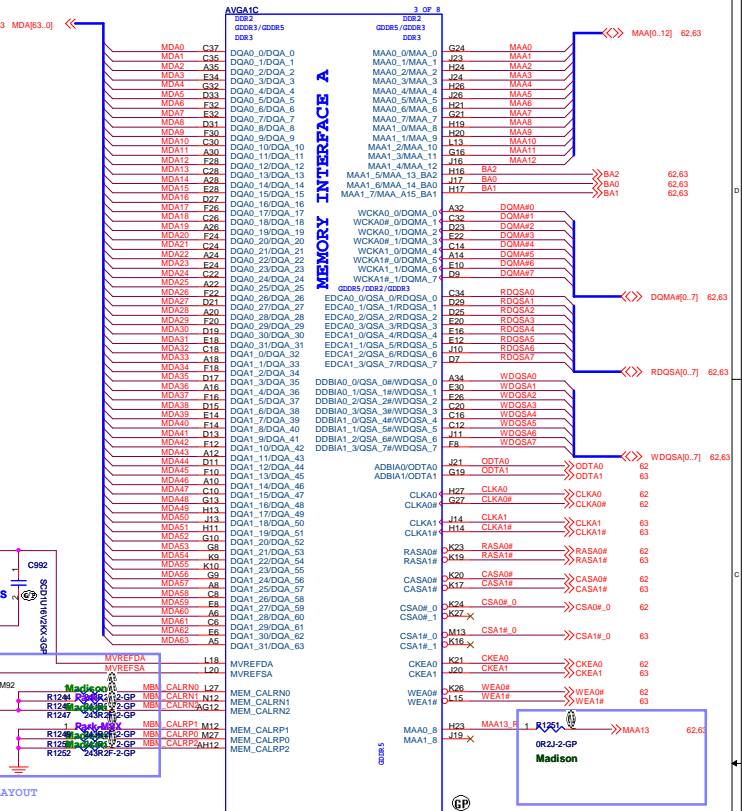


STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X= DESIGN DEPENDANT NA= NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCI FULL TX OUTPUT SWING Transmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	1
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIe GEN2 ENABLED 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s	1
AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	
ROMSO	GPIO8	BF CLK PM EN Serial ROM Output from ROM	0
ROMSI	GPIO9	VGA ENABLED Serial ROM Input to ROM	0
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size	X X X

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X= DESIGN DEPENDANT NA= NOT APPLICABLE
PWRCTRL[1,0]	GPIO[15,20]	Power control signals to control the core voltage regulator	
BB_EN	GPIO21	Back Bias (body bias) which minimizes power consumption in battery modes. 0V = Disable 3D3V = Enable	0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00: No audio function 01: Audio for DisplayPort and HDMI (if adapter is detected) 10: Audio for DisplayPort only 11: Audio for both DisplayPort and HDMI	1
CCBYPASS	GENERIC		0

HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

STRAPS	PIN	DESCRIPTION
GPIO	DVPPDATA[23:20] (Internal PD)	Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V). The signals above can be left unconnected if not used.



Designator	For M96-M2	For Mannheim	M92-M2
R_MEM_1	R628	4.7K	DY
R_MEM_2	R1230	0R	680R
R_MEM_3	R1269	4.7K	10K
C_MEM	C961	1nF	68pF

AMD RESERVED CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
H2SYNCR, GENERIC			
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
GPIO_28_TDO, GPIO21_BB_EN			

If BIOS_ROM_EN (GPIO22) = 0				If BIOS_ROM_EN (GPIO22) = 1			
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100			
256MB	x001		M25P10A	0101			
64MB	x010		M25P20	0101			
32MB	x		M25P40	0101			
512MB	x	Chingis (formerly PMC)	M25P80	0101			
1GB	x						
2GB	x						
4GB	x		Pm25LV512A	0100			
			Pm25LV010A	0101			

71.MDS0N.M01

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

File: Madison Memory / Straps

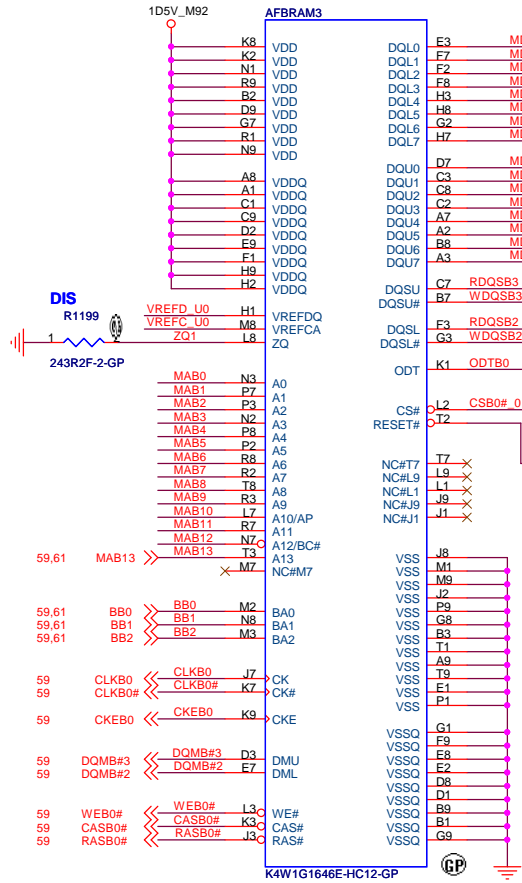
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GDDR3



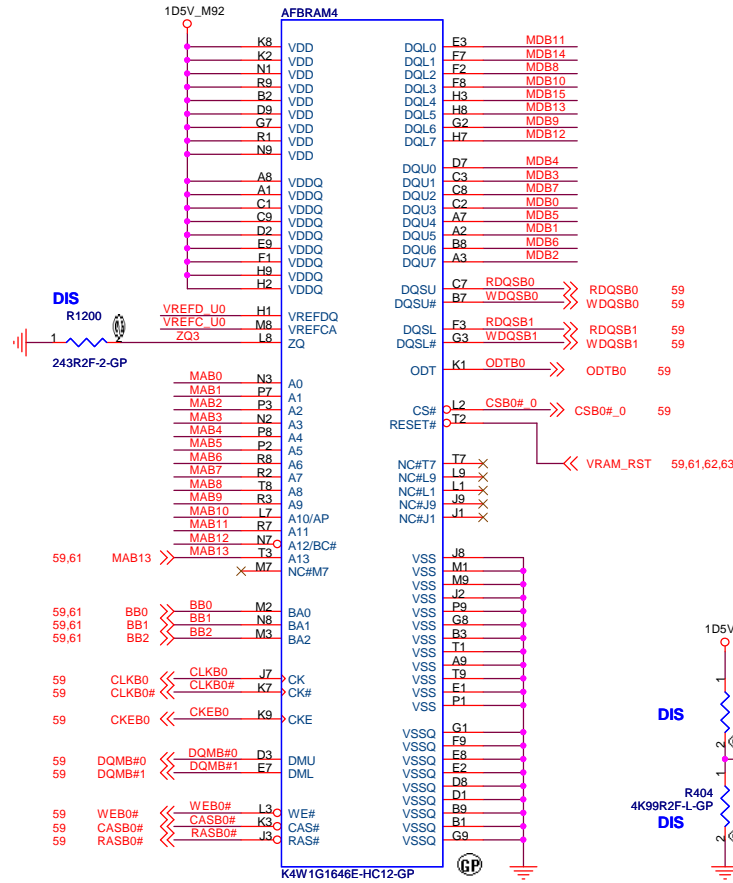
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2ND = 72.51G63.C0U

SAMSUNG 1ST=72.41164.H0U

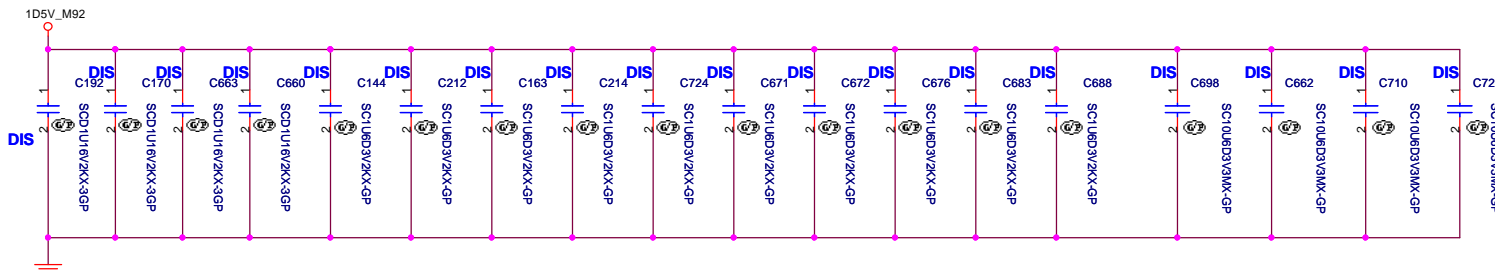
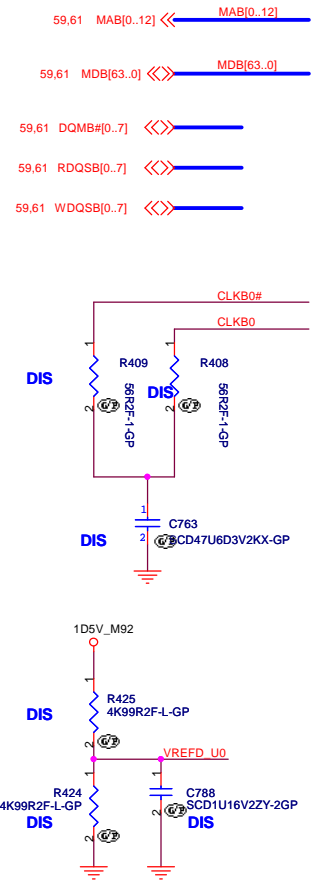
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DIS

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2ND = 72.51G63.C0U

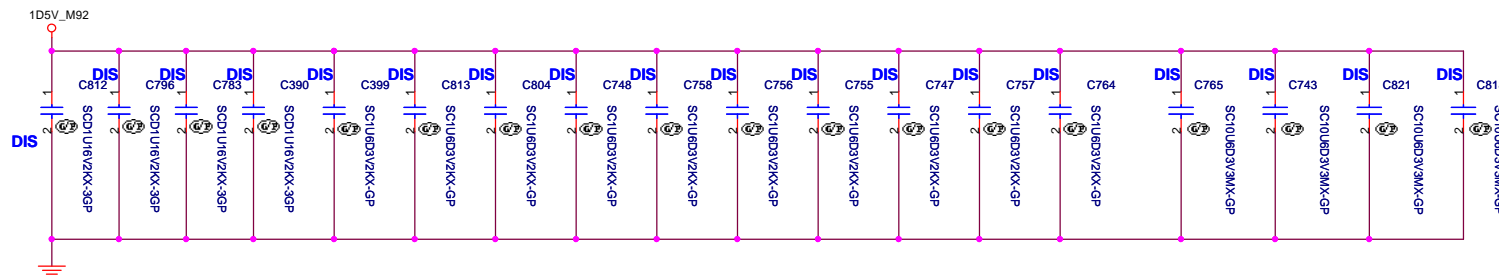
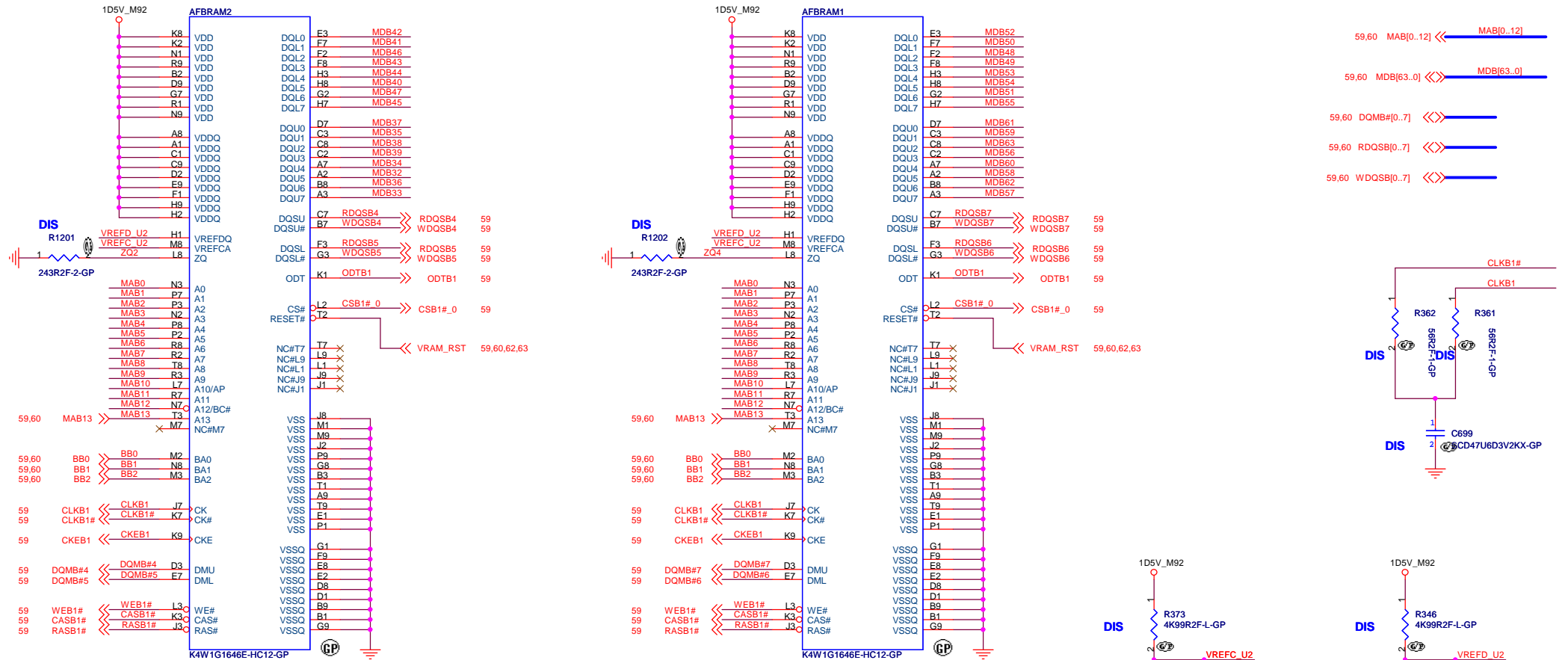


JV50-TR8

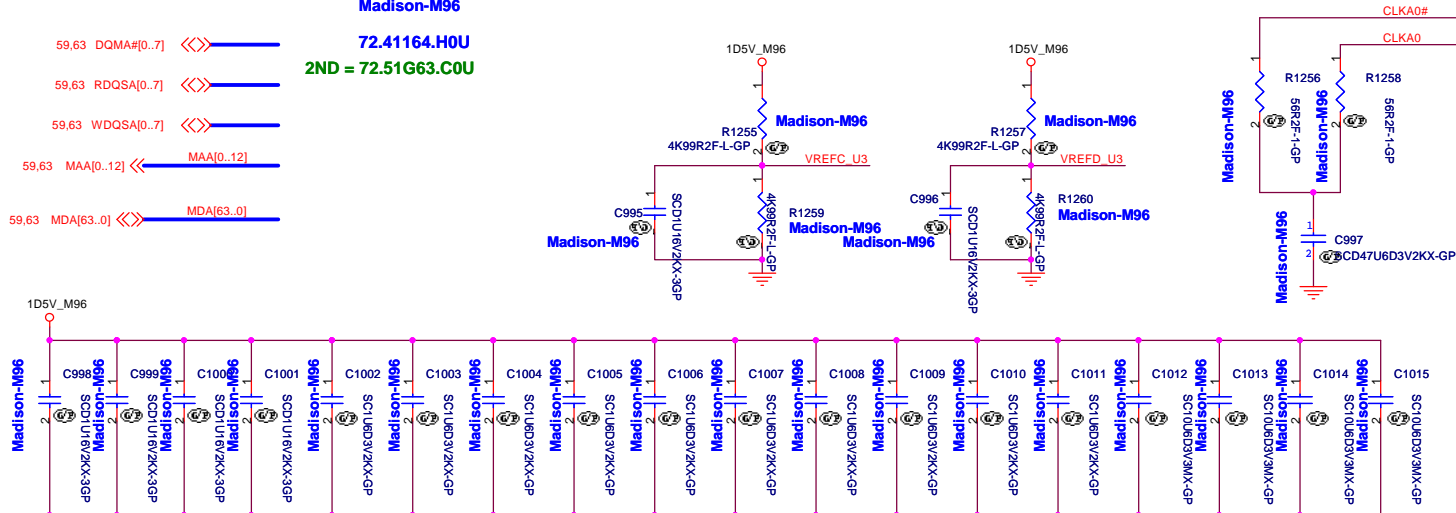
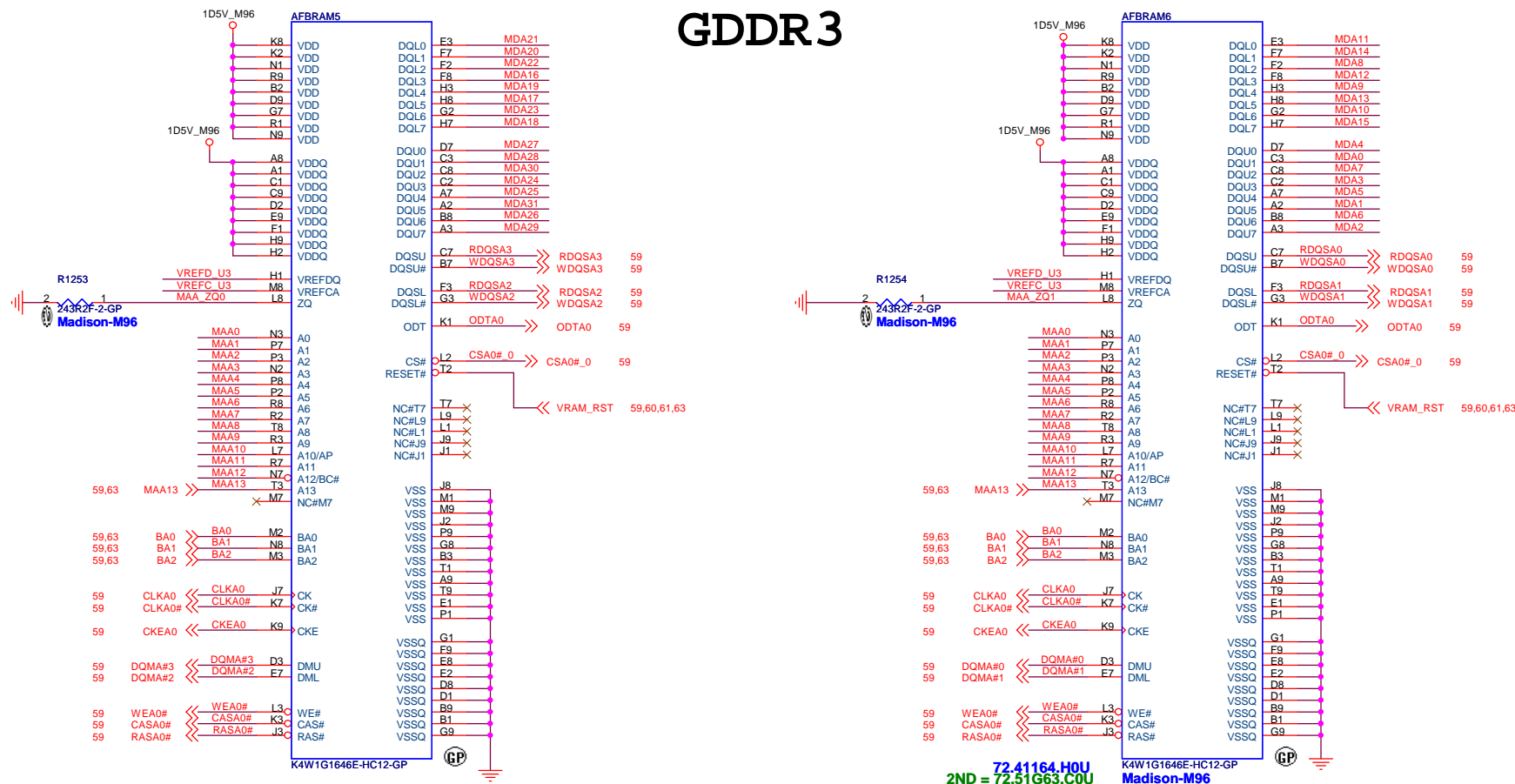
緯創資通 Wistron Corporation
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GDDR3



GDDR 3



GDDR3

